STIC Search Report
EIC 2600

USPTO

STIC Database Tracking Number: 131296

TO: John Villecco
Location: CPK2-6B42
Art Unit : 2612
Thursday, September 02, 2004

Case Serial Number: 09/883,990

From: Samir Patel
Location: EIC 2600
PK2-3C03
Phone: 306-0254

Samir.patel@uspto.gov

Search Notes

Dear Examiner, Date:-09/02/04

Please find attached the search results for 09/883990. I used the search strategy I talked to you. I searched the standard Dialog files, IEEE, DTIC and the internet.

If you would like a re-focus please let me know.

Thank You
Samir Patel

Access DB# 1312

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: John Villecco Examiner # : 78676 Date: 8/31/04
Art Unit: 2612 Phone Number 305-1460 Serial Number: 09/883990
~~Mail Box~~ Location: CPK2 6B42 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept o utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: Semiconductor integrated circuit

Inventors (please provide full names): Eiji Koyama

Earliest Priority Filing Date: 6/20/2000

****For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with th appropriate serial number.***

Integrated circuit for image sensor which reduces noise between an analog and digital circuit by phase shifting clock signals. Keywords: phase, shift, noise, analog, digital, clock

9:30

****

STAFF USE ONLY	Type of Search	Vendors and cost where applicable
Searcher: Patel Samir	NA Sequence (#)	STN
Searcher Phone #: 306-0254	AA Sequence (#)	Dialog ✓
Searcher Location: PK2-9C03	Structure (#)	Questel/Orbit
Date Searcher Picked Up: 9:00A.M 09/02	Bibliographic ✓	Dr.Link
Date Completed: 3:20P.M 09/02	Litigation	Lexis/Nexis
Searcher Prep & Review Time: 190	Fulltext ✓	Sequence Systems
Clerical Prep Time: 78	Patent Family	WWW/Internet
Online Time:	Other	Other (specify)

```
File   2:INSPEC 1969-2004/Aug W4
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Aug W4
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/Aug W4
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Aug W5
         (c) 2004 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/Jul
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Aug W5
         (c) 2004 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2004/Aug W1
         (c)2004 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Jul
         (c) 2004 The HW Wilson Co.
File 144:Pascal 1973-2004/Aug W4
         (c) 2004 INIST/CNRS
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 239:Mathsci 1940-2004/Oct
         (c) 2004 American Mathematical Society
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
File 603:Newspaper Abstracts 1984-1988
         (c)2001 ProQuest Info&Learning
File 483:Newspaper Abs Daily 1986-2004/Sep 01
         (c) 2004 ProQuest Info&Learning
File 248:PIRA 1975-2004/Aug W4
         (c) 2004 Pira International

Set     Items   Description
S1      68835    (SEMICONDUCTOR?? OR SEMI()CONDUCTOR??? OR SOLID()STATE?? OR
                  SOLIDSTATE?? OR IC OR CHIP?? OR CIRCUIT??) AND (IMAGE??(2N)S-
                 ENS??? OR CCD OR IMAGE()PICK??? OR PHOTOCELL?? OR PHOTODETECT-
                 OR?? OR PHOTOSENSOR??)
S2      32493   ANALOG(2N)(CIRCUIT?? OR IC OR CHIP??)
S3      91234   DIGITAL(2N)(CIRCUIT?? OR IC OR CHIP??)
S4     138333   PHASE(5N)SHIFT???
S5        542   (S2 AND S3) AND CLOCK??
S6      94010   NOISE??(2N)(REDUC???? OR MINIMIZ??? OR SUPPRESS???)
S7        324   S1 AND S2 AND S3
S8          1   S7 AND S4
S9         12   S2 AND S3 AND S4 AND S5
S10         8   RD (unique items)
S11        15   S1 AND S2 AND S3 AND S6
S12         0   S11 AND S4
S13       500   AU=(KOYAMA E? OR KOYAMA, E?)
S14         6   S13 AND S1
S15         3   RD (unique items)
S16      2380   S1 AND ANALOG?? AND DIGITAL??
S17        10   S16 AND S4
S18         0   S17 AND S5
S19         9   RD S17 (unique items)
S20         8   S19 NOT (S8 OR S10)
```

8/3,K/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05245925 JICST ACCESSION NUMBER: 02A0706922 FILE SEGMENT: JICST-E
New Deployment of Digital **Vision** Chip .
ISHIKAWA MASATOSHI (1); KOMURO TAKASHI (1); KAGAMI SHINGO (1)
(1) Univ. of Tokyo
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 2002, VOL.102,NO.234(ICD2002 35-45), PAGE.23-28, FIG.10, TBL.1, REF.10
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.37+ 621.382.2/.3.049.77 681.3:621.397.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

New Deployment of Digital **Vision** Chip .
ABSTRACT: A vision **chip** is a device in which processing **circuits** are attached to each pixel of an **image sensor** and it can perform ultra high speed image processing owing to no need of transmitting image data. Though most of existing vision **chips** ever studied consists of **analog circuits** , the authors have been studied **digital** vision **chips** which introduce **digital circuits** for processing aiming to perform more flexible and high level processing. Recently the study has progressed remarkably and the **phase** is **shifting** from the basic principle to practical use. In this paper such new study results are...
...DESCRIPTORS: **image sensor** ; ...

... **semiconductor chip** ;
...BROADER DESCRIPTORS: **image pickup** apparatus...

...integrated **circuit** ; ...

...micro **circuit** ; ...

... **solid state circuit** parts...

... **circuit** component...

... **chip**

10/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6629444 INSPEC Abstract Number: B2000-08-6430C-005
Title: A dynamically configurable multiformat PSK demodulator for digital HDTV using broadcasting-satellite
Author(s): Arita, E.; Fujiwara, T.; Nishiyama, K.; Maeno, A.; Matsunami, Y.; Nakamura, M.; Machida, H.; Murakami, S.; Takeuchi, S.; Nakayama, H.; Yoshimoto, M.
Author Affiliation: Inf. Technol. R&D Center, Mitsubishi Electr. Co., Kyoto, Japan
Conference Title: 2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056) p.72-3, 448
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 496 pp.
ISBN: 0 7803 5853 8 Material Identity Number: XX-2000-00786
U.S. Copyright Clearance Center Code: 0 7803 5853 8/2000/$10.00
Conference Title: 2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers
Conference Date: 7-9 Feb. 2000 Conference Location: San Francisco, CA, USA
Language: English
Subfile: B
Copyright 2000, IEE
...Abstract: year 2000. The Japanese BS digital system has one of three different modulation formats (binary **phase shift** keying (BPSK), quadrature PSK (QPSK), and 8PSK), dynamically selected according to transmission and multiplexing configuration...

... which employs a flexible carrier-recovery system achieving dynamically configurable multi-format demodulation, and a **clock phase** compensator and carrier **phase shifter** cancelling the poor performance of the **analog** front-end **circuit** .
...Descriptors: mixed analogue- **digital** integrated **circuits** ; ...

... **phase shift** keying...

...quadrature **phase shift** keying
...Identifiers: binary **phase shift** keying...

... **clock** phase compensator...

...carrier **phase shifter**

10/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6418542 INSPEC Abstract Number: B2000-01-6250G-010
Title: A single- chip **universal** digital **satellite receiver with 480-MHz IF input**
Author(s): Kwentus, A.Y.; Pai, P.; Jaffe, S.; Gomez, R.; Tsai, S.; Kwan, T.; Hing-Tsun Hung; Shin, Y.J.; Hue, V.; Cheung, D.; Khan, R.A.; Ward, C.M. ; Mong-Kai Ku; Choi, K.; Searle, J.; Bult, K.; Cameron, K.; Demas, J.; Reames, C.; Samueli, H.

Author Affiliation: Broadcom Corp., Irvine, CA, USA
Journal: IEEE Journal of Solid-State Circuits Conference Title: IEEE J. Solid-State Circuits (USA) vol.34, no.11 p.1634-46
Publisher: IEEE,
Publication Date: Nov. 1999 Country of Publication: USA
CODEN: IJSCBC ISSN: 0018-9200
SICI: 0018-9200(199911)34:11L.1634:SCUD;1-V
Material Identity Number: I022-1999-012
U.S. Copyright Clearance Center Code: 0018-9200/99/$10.00
Conference Title: 1999 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition
Conference Sponsor: IEEE Solid State Circuits Soc.; IEEE San Francisco Sect., Bay Area Council; Univ. PA
Conference Date: 15-17 Feb. 1999 Conference Location: San Francisco, CA, USA
Language: English
Subfile: B

Title: A single- chip **universal** digital **satellite receiver with 480-MHz IF input**
Abstract: This paper presents a complete single- **chip** universal **digital** satellite receiver supporting all current DBS system standards. The mixed-signal device accepts a modulated...

...at up to 90 Mbps and delivers a demodulated, error-corrected output data stream. The **IC** features an **analog** front end with 480-MHz intermediate frequency downconversion and dual 8-bit analog-to-digital...

... concatenated Viterbi/Reed-Solomon forward error correction decoder with on-chip deinterleaver RAM. All required **clocks** are generated on chip from a single reference crystal. The chip contains 1.2 million...
...Descriptors: mixed analogue- **digital** integrated **circuits** ; ...

...quadrature **phase** **shift** keying

10/3,K/3 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1098422 NTIS Accession Number: AD-A138 313/2
Single Circuit Board Implementation of a Digitally Compensated SAW Oscillator (DCSO)
(Master's thesis)
McGuire, J. W.
Air Force Inst. of Tech., Wright-Patterson AFB, OH. School of Engineering.
Corp. Source Codes: 000805002; 012225
Report No.: AFIT/GE/EE/83D-44
Dec 83 128p
Languages: English Document Type: Thesis
Journal Announcement: GRAI8411
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A07/MF A01

... results. The portion of the circuit consisting of the D/A converter, op amp, and **phase shifter** was tested. For various addresses programmed on the D/A converter inputs, which simulated the output from the two EPROMs, a total **phase shift** of 107 degrees was obtained from the **phase shift** circuit. The thermometer and **clock** paths of the SAW device were made to oscillate at their respective resonant frequencies by introducing the proper amounts of **phase shift** and attenuation into the feedback loops. The thermometer and **clock** resonant frequencies were 309 MHz and 298 MHz respectively.
Descriptors: **Clocks** ; *Surface acoustic wave devices; *Digital systems; *Crystal oscillators; *Surface waves; *Acoustic waves; **Phase shift circuits** ; **Digital** to **analog** converters; Resonant frequency; Compensation; Feedback; Attenuation; Temperature; Circuit boards; Parts; **Phase shift** ; Thermometers; Paths; Off the shelf equipment; Very high frequency; Operational amplifiers; Circuits; Loops; Oscillators; Theses
Identifiers: **Clock** loops; DCSO(Digitally Compensated SAW Oscillators) Tunable **clocks**); NTISDODXA

10/3,K/4 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06156999 E.I. No: EIP02417129645
Title: Universal low-jitter level shifter drives high-performance ADCs
Author: LeBoeuf, Robert
Corporate Source: National Semiconductor Corp. East Coast Labs Div., Salem, NH 03079, United States
Source: Electronic Design v 50 n 19 Sep 16 2002. p 91-92
Publication Year: 2002
CODEN: ELODAW ISSN: 0013-4872
Language: English

...Abstract: digital converters (ADC) was designed. The circuit was an excellent source for generating low-jitter **clocks** . It was also applicable for designing system which required **clocks** to be level-shifted, reshaped or converted from single ended to differential with a minimum...
Descriptors: **Digital circuits** ; **Analog** to **digital** conversion; Square wave generators; Digital communication systems; Timing circuits; **Phase shift** ; Jitter; Logic gates; Electric impedance; Bit error rate; Digital signal processing; Electric lines; Waveform analysis

10/3,K/5 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04868044 E.I. No: EIP97113912669
Title: Proceedings of the 1997 Symposium on VLSI Circuits
Author: Anon (Ed.)
Conference Title: Proceedings of the 1997 Symposium on VLSI Circuits
Conference Location: Kyoto, Jpn Conference Date: 19970612-19970614
E.I. Conference No.: 47243
Source: IEEE Symposium on VLSI Circuits, Digest of Technical Papers 1997. IEEE, Piscataway, NJ, USA,97CH36115. 124p
Publication Year: 1997
CODEN: 85PXA5

Language: English

Descriptors: VLSI circuits; CMOS integrated **circuits** ; Microprocessor **chips** ; **Analog** to **digital** conversion; Transceivers; Reduced instruction set computing; Timing circuits; Random access storage; Modulators; Computer simulation

...Identifiers: interfaces; Dummy carry method; Flash memory; Chain ferroelectric random access memory (CFRAM); Inductor capacitor (LC) **phase shifters** ; Reduced **clock** swing flip flops (RCSFF); EiRev

10/3,K/6 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04530658 E.I. No: EIP96103367904

Title: Advanced two IC chipset for DVB on satellite reception

Author: Haas, M.; Kuttner, F.; Frieling, F.; Hobbach, G.; Kriedt, H.; Mueller, K.; v. Reventlow, C.

Corporate Source: Siemens AG, Villach, Austria

Source: IEEE Transactions on Consumer Electronics v 42 n 3 Aug 1996. p 341-345

Publication Year: 1996

CODEN: ITCEDA ISSN: 0098-3063

Language: English

...Abstract: I/Q demodulator with on-chip AGC and a MOS QPSK processor device with ADC, **clock** and carrier recovery Viterbi- and RS forward error correction. (Author abstract) 1 Refs.

Descriptors: Satellite communication systems; Radio receivers; Demodulators; Gain control; Error correction; CMOS integrated **circuits** ; **Analog** to **digital** conversion; **Phase shift** keying

10/3,K/7 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03966746 E.I. No: EIP94111436618

Title: Power metering ASIC with a sigma-delta-based multiplying ADC

Author: t?Eynde, F. Op

Corporate Source: Mietec Alcatel, Brussels, Belgium

Conference Title: Proceedings of the 1994 IEEE International Solid-State Circuits Conference

Conference Location: San Francisco, CA, USA Conference Date: 19940216-19940218

E.I. Conference No.: 20737

Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1994. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. p 186-187

Publication Year: 1994

CODEN: DTPCDE ISBN: 0-7803-1845-5

Language: English

...Abstract: a fully-electronic equivalent. The ASIC schematic is shown. Support circuits such as bandgap reference, **clock** generation logic and the power-on-reset are not shown. Three second-order sigma-delta...

...signs of v(t) and i(t). Their outputs allow measurement of line frequency and **phase shift** . One comparator contains two autozeroed chopped comparator stages for 3 mu V, sensitivity. For interfacing...
Descriptors: Electric power measurement; Electric measuring instruments; Integrated **circuits** ; **Analog** to **digital** conversion; Multiplying **circuits** ; Electronic equipment; Modulators; Design; Schematic diagrams

10/3,K/8 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

01720194 Genuine Article#: HV420 No. References: 232
Title: CONTINUOUSLY VARIABLE GIGAHERTZ PHASE - SHIFTER **IC COVERING MORE THAN ONE FREQUENCY DECADE**
Author(s): SCHMIDT L; REIN HM
Corporate Source: RUHR UNIV BOCHUM,INST ELECTR/W-4630 BOCHUM//GERMANY/
Journal: IEEE JOURNAL OF SOLID-STATE CIRCUITS, 1992, V27, N6 (JUN), P 854-862
Language: ENGLISH Document Type: ARTICLE (Abstract Available)

Title: CONTINUOUSLY VARIABLE GIGAHERTZ PHASE - SHIFTER **IC COVERING MORE THAN ONE FREQUENCY DECADE**
Abstract: A monolithic integrated silicon bipolar circuit is described, which allows **phase shifting** of arbitrarily shaped **clock** signals by 0 to -2-pi within a frequency range, from about 60 MHz to...

...adjusted by a single potentiometer or by an externally applied voltage. The wide frequency and **phase - shifting** ranges were achieved by a new mainly **digital circuit** principle. The temperature coefficient of the phase can be adjusted within a specific range. The...
...Research Fronts: IN GAAS-GA1-XALXAS QUANTUM-WELLS)
90-0653 001 (LINEAR CMOS FLOATING RESISTOR; CURRENT-MODE **CIRCUITS** ; ALGORITHMIC **ANALOG** -TO-DIGITAL CONVERTERS; CONTINUOUS-TIME FILTERS)

5/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

04033873 INSPEC Abstract Number: B9201-7230G-010
Title: **High sensitivity** CCD image sensor **for normal and mirror images**
Author(s): **Koyama, E.** ; Masui, T.; Jun'ichi Nakai; Misawa, K.; Shun'ichi Naka
Journal: Sharp Technical Journal no.50 p.29-32
Publication Date: Sept. 1991 Country of Publication: Japan
CODEN: STEJD9 ISSN: 0285-0362
Language: Japanese
Subfile: B

Title: **High sensitivity** CCD image sensor **for normal and mirror images**
Author(s): **Koyama, E.** ; Masui, T.; Jun'ichi Nakai; Misawa, K.; Shun'ichi Naka
...Abstract: growing market of camcorders requires small size, high sensitivity and highly improved functions for a **solid - state image sensor** . To meet these demands, the authors have developed a 1/3-inch format 542(H)*492(V) element **CCD image sensor** with improved sensitivity by microlens technique. This paper describes both the process technique for high...
Descriptors: **CCD image sensors ;**
...Identifiers: **CCD image sensor ;**

15/3,K/2 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02690458 JICST ACCESSION NUMBER: 96A0223637 FILE SEGMENT: JICST-E
Core Devices. 1/5-Type 220K Pixel CCD **Area Sensor with 5V-Single Power Supply.**
KOYAMA EIJI (1); YOSHIZAWA KAZUNORI (1); YAMAMOTO KENGO (1); OKADA KOJI (1); ADACHI HIROSHI (1); KAWASAKI TAKAYUKI (1); INOUE TSUGUHISA (1); AKAIKE EIICHI (1); MISAWA KIYOTOSHI (1)
(1) Shapu ICKaise
Shapu Giho(Sharp Technical Journal), 1995, NO.63, PAGE.34-37, FIG.6, TBL.2, REF.5
JOURNAL NUMBER: G0524AAD ISSN NO: 0285-0362 CODEN: STEJD
UNIVERSAL DECIMAL CLASSIFICATION: 621.397.61
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

Core Devices. 1/5-Type 220K Pixel CCD **Area Sensor with 5V-Single Power Supply.**
KOYAMA EIJI (1); YOSHIZAWA KAZUNORI (1); YAMAMOTO KENGO (1); OKADA KOJI (1); ADACHI HIROSHI (1); KAWASAKI TAKAYUKI (1); INOUE TSUGUHISA (1); AKAIKE EIICHI...
(1)
ABSTRACT: In addition to a series of unique **CCD** 's with two power supplies (+5V, +12V), we have newly developed 1/5 type 220K pixel **CCD** area sensor driven only by single power supply of +5V Compared with

conventional **CCD** with four power supplies, our new device enables camera system not only to reduce power...

...small size and low cost for multimedia use. This paper describes technologies essential to drive **CCD** with 5V-single power supply and demonstrates how this device simplifies camera system. (author abst.)
DESCRIPTORS: **image sensor** ; ...

...driving **circuit** ;
BROADER DESCRIPTORS: **image pickup** apparatus...

... **semiconductor** device...

... **solid state** device...

... **circuit** ;

15/3,K/3 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01401082 JICST ACCESSION NUMBER: 91A0756002 FILE SEGMENT: JICST-E
A Single-Output CCD Image Sensor **for Normal and Mirror Images.**
KOYAMA EIJI (1); MAEDA TADANOBU (1); WATANABE TAKASHI (1); MISAWA KIYOTOSHI (1); NAKANO SHUN'ICHI (1)
(1) Sharp Corp.
Terebijon Gakkai Nenji Taikai Koen Yokoshu(Proceedings of the ITE Annual Convention), 1991, VOL.1991, PAGE.31-32, FIG.3, REF.1
JOURNAL NUMBER: S0530ABD
UNIVERSAL DECIMAL CLASSIFICATION: 621.382:537.222 621.397.61
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication

A Single-Output CCD Image Sensor **for Normal and Mirror Images.**
KOYAMA EIJI (1); MAEDA TADANOBU (1); WATANABE TAKASHI (1); MISAWA KIYOTOSHI (1); NAKANO SHUN'ICHI (1)
...DESCRIPTORS: **image sensor**
...BROADER DESCRIPTORS: **image pickup** apparatus...

... **semiconductor** device...
... **solid state** device
?

? type/3,k/all

20/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7604787 INSPEC Abstract Number: B2003-06-7230G-023, C2003-06-5530-003
Title: A continuous time pattern recognition retina
Author(s): Cathebras, G.; Navarro, D.; Aubreton, O.; Bellach, B.; Gorria, P.; Lamalle, B.; Lew Yan Voon, L.F.C.
Author Affiliation: LIRMM, Univ. Montpellier II, France
Conference Title: ESSCIRC 2002. Proceedings of the 28th European Solid-State Circuit Conference p.719-22
Editor(s): Baschirotto, A.; Malcovati, P.
Publisher: Univ. Bologna, Bologna, Italy
Publication Date: 2002 Country of Publication: Italy xvii+846 pp.
ISBN: 88 900847 9 0 Material Identity Number: XX-2003-00077
Conference Title: ESSCIRC 2002. Proceedings of the 28th European Solid-State Circuit Conference
Conference Date: 24-26 Sept. 2002 Conference Location: Firenze, Italy
Language: English
Subfile: B C
Copyright 2003, IEE

...Abstract: stored in the sensor's pixels. During the recognition phase, the retina calculates, in an **analog** way and in continuous time, the zero displacement intercorrelation of the current image with the...
... are output as currents. By comparing these currents to expected values, determined during the programming **phase** , a **shift** of the pattern or a difference between the observed and programmed pattern can be detected. A 100*100 pixels validation **chip** was fabricated using a standard CMOS triple level metal 0.6 mu m process. Characterization...
Descriptors: CMOS **image** **sensors** ; ...

...mixed **analogue** - **digital** integrated **circuits** ;
...Identifiers: **image** **sensor** ; ...

... **analog** / **digital** signal processing

20/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6943201 INSPEC Abstract Number: B2001-07-7230-017, C2001-07-3240D-004
Title: The next generation of position sensing technology. II. Differential displacement and linear capabilities
Author(s): Madni, A.M.; Vuong, J.B.; Wells, R.F.
Author Affiliation: BEI Technol. Inc., Sylmar, CA, USA
Journal: Sensors vol.18, no.4 p.61-5
Publisher: Advanstar Communications,
Publication Date: April 2001 Country of Publication: USA
CODEN: SNSRES ISSN: 0746-9462
SICI: 0746-9462(200104)18:4L.61:NGPS;1-Q
Material Identity Number: P585-2001-013
Language: English
Subfile: B C
Copyright 2001, IEE

...Abstract: linearity of better than +or-0.5% over 360 degrees of rotation. The measurement of **phase shift**, rather than the magnitude of the coupling signal, to determine the angular position gives the...

... to mechanical misalignment of the rotating components and makes it conducive to mass production. The **analog** and **digital** signal processing electronics can be readily converted to an ASIC. The sensor, which does not use any permanent magnets, LEDs, or **photodetectors**, lends itself to the high-volume, low-cost, and high-reliability requirements of the automotive ...

Descriptors: **analogue** processing **circuits** ; ...

... **digital** signal processing **chips** ;

...Identifiers: **phase shift** measurement...

... **digital** signal processing electronics...

... **analog** signal processing electronics...

... **photodetectors** ;

20/3,K/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

5931911 INSPEC Abstract Number: B9807-1350H-012

Title: Multifunctional integration using HEMT technology

Author(s): Schlechtweg, M.; Verweyen, L.; Haydl, W.; Thiede, A.; Lang, M. ; Leber, P.; Hurm, V.; Jakobus, T.; Bronner, W.; Hulsmann, A.; Hornung, J.; Wang, Z.

Author Affiliation: Fraunhofer Inst. for Appl. Solid State Phys., Freiburg, Germany

Conference Title: ESSDERC '97. Proceedings of the 27th European Solid-State Device Research Conference p.57-74

Editor(s): Grunbacher, H.

Publisher: Editions Frontieres, Paris, France

Publication Date: 1997 Country of Publication: France xvi+767 pp.

ISBN: 2 86332 221 4 Material Identity Number: XX97-02325

Conference Title: 27th European Solid-State Device Research Conference (ESSDERC '97)

Conference Date: 22-24 Sept. 1997 Conference Location: Stuttgart, Germany

Language: English

Subfile: B

...Abstract: high frequency applications using HEMT technology. The following topics will be discussed: combination of different **circuit** functions for complex millimeter-wave ICs, monolithic integration of **analog** and **digital** functions, integrated microwave and **digital** functions, integration of optical and electronic components in OEICs. In the first part, interconnection techniques...

... relevant for multifunctional integration. In the following sections we will present different examples for multifunctional **circuits** which comprise 77 GHz automotive radar, 15 GHz and 34 GHz phase locked loop oscillators, a 35 GHz **phase shifter**, and high speed optoelectronic

receiver **circuits** based on MSM and PIN **photodetectors** .
...Descriptors: HEMT integrated **circuits** ; ...

...millimetre wave **phase shifters** ;
...Identifiers: different **circuit** functions...

...complex millimeter-wave **IC** ; ...

... **digital** functions...

... **analog** functions...
...integrated microwave and **digital** functions...

... **phase shifter** ; ...

...high speed optoelectronic receiver **circuits** ; ...

...PIN **photodetectors** ; ...

...MSM **photodetectors** ; ...

...transmitter **chip** ;

20/3,K/4 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1468534 NTIS Accession Number: NTN89-0838
Optically-Controlled Microwave Devices and Circuits : **Optical control increases speed and reduces the bulk of interconnections**
(NTIS Tech Note)
National Aeronautics and Space Administration, Washington, DC.
Corp. Source Codes: 011249000
Oct 89 1p
Languages: English
Journal Announcement: GRAI9001
FOR ADDITIONAL INFORMATION: Detailed information about the technology described may be obtained by ordering the NTIS report, NTIS order number N87-23900/NAC, price code A02.
NTIS Prices: Not available NTIS

Optically-Controlled Microwave Devices and Circuits : **Optical control increases speed and reduces the bulk of interconnections**
... on the responses of GaAs/GaAl/As high-electron-mobility transistors (HEMTs) and GaAs metal/ **semiconductor** field-effect transistors (MESFETs) to light. Such devices have been used to detect radio-frequency...

... optical and microwave functions on a single GaAs substrate is expected to provide light-weight **digital** and **analog** links for control and the distribution of signals. In a typical device, light from optical fibers would be coupled through aligners to integrated **photodetectors** on a GaAs monolithic microwave integrated **circuit** : Optically-controlled microwave devices (interdigitated **photodetectors**) can demodulate radio-frequency signals carried by optical signals. They can also detect and amplify **digital** signals at rates of gigabits per second to control the functions of **phase shifters** and the gains of amplifiers in transmitting modules.

20/3,K/5 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS

1284335 NTIS Accession Number: AD-A176 097/4
Solid State **Research**
(Quarterly technical rept. 1 Nov 85-31 Jan 86)
McWhorter, A. L.
Massachusetts Inst. of Tech., Lexington. Lincoln Lab.
Corp. Source Codes: 009875001; 207650
Sponsor: Electronic Systems Div., Hanscom AFB, MA.
Report No.: 1986-1; ESD-TR-86-020
15 Feb 86 78p
Languages: English
Journal Announcement: GRAI8709
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A05/MF A01

Solid State **Research**
... Dimensional Arrays of High Power GaInAsP/In P Surface Emitting Diode Lasers; Intermodulation Measurements of **Semiconductor** Diode Lasers; Room Temperature CW Operation of a Ti:Al2O3 Laser; Er: YAG Laser Developement...
... Silicon on Insulator Films; Radiation Hardened Silicon on Insulator JFETs; Ti Doped Semi-insulating InP; **CCD** Vector Matrix Product Device; A Low Loss Ku Band Monolithic **Analog Phase Shifter** ; Electron Beam Programming of CMOS **Digital** Systems; Noise Properties of Quantum Well Structure; Technologies for Optical Interconnects; Heterodyne Imaging of a ...
Descriptors: **Semiconductor** lasers; * **Solid state** physics; Monolithic structures(Electronics); Signal processing; Antennas; Associative processing; Electron beams; Emission; Heterodyning; High power; Images; Intermodulation; Matched filters; Measurement; Noise; Nonlinear systems; Optical images; Radiation hardening; Recrystallization; Room temperature; **Semiconductor** diodes; Silicon; Strip transmission lines; Structural properties; Surfaces; Zone melting; Heterojunctions; Gallium arsenides; Indium phosphides; Surface acoustic wave devices; Yag lasers; Doping; Europium; Aluminum oxides; Titanium; Field effect transistors; **Photodetectors** ; Quantum electronics; Charge coupled devices; Arrays

20/3,K/6 (Item 3 from file: 6)
DIALOG(R)File 6:NTIS

0282538 NTIS Accession Number: AD-883 359/XAB
Charge-Coupled Circuits
(Scientific Rept. no. 2, 1 Nov 69-31 Oct 70)
Kosonocky, W. F.
RCA Labs., Princeton, N.J.
Corp. Source Codes: 299000
Report No.: AFCRL-71-0121
Feb 71 65p
Journal Announcement: GRAI7118

Distribution Limitation now Removed.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A04/MF A01

Charge-Coupled Circuits
This report describes the operation and the applications of charge-coupled shift registers for **analog** and **digital** signals. Silicon-gate construction is proposed for achieving high-performance, high-density structures, and also...
... drift field due to an uneven charge distribution is considered. Simple signal-regeneration stages for **digital** charge-coupled shift registers are described, and their operation is demonstrated by charge-coupled **circuits** made by a p-MOS process. A charge-transfer efficiency of about 99.6% per electrode at a clock frequency of 1 MHz was obtained in the operation of 3-**phase** 8-bit **shift** registers made by the p-MOS process. The feasibility of self-scanning charge-coupled **photosensor** arrays for video signal is briefly discussed. The study shows that charge-coupled devices can be used for high-packing-density **digital** shift registers or memories. Logic **circuits** that operate with electrical or optical inputs can be made with charge-coupled devices. Such a charge-coupled **circuit** is expected to have a packing density of about 1 sq. mil of silicon area...
Descriptors: Shift registers; *Integrated **circuits** ; *Thin film storage devices; *Gates(**Circuits**); Coupling **circuits** ; Carriers(**Semiconductors**); **Analog** systems; Semiconducting films; Electronic scanners; Photodiodes ; Delay lines; Images; **Digital** systems; Phase(Electronics); Pulse systems ; Computer logic; Clocks; Medium frequency; Logic **circuits** ; Video signals ; Resolution; Electric fields; Diffusion; Mobility; Silicon compounds; Silicon; Aluminum; Oxides; **Circuit** interconnections; Performance(Engineering)
Identifiers: **Semiconductor** memories; * **Analog** shift registers; Mos(Metal Oxide **Semiconductors**); Metal oxide **semiconductors** ; Depletion region; Charge coupled devices; Transparent electrodes; Optical arrays; Dynodes; Floating electrodes; NTISAF

20/3,K/7 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04512229 E.I. No: EIP96043156548
Title: HgCdTe infrared linear arrays for 3-5- and 8-12-um wavelength regions
Author: Darchuk, Sergey D.; Derkach, Y.P.; Kononenko, Y.G.; Petryakov, V.A.; Reva, V.P.; Sizov, Fiodor F.; Tetyorkin, Vladimir V.
Corporate Source: Inst. of Semiconductor Physics, Kiev, Ukraine
Conference Title: Int. Conference on Optical Diagnostics of Materials and Devices for Opto-, Micro-, and Quantum Electronics
Conference Location: Kiev, Ukraine Conference Date: 19950511
E.I. Conference No.: 22513
Source: Proceedings of SPIE - The International Society for Optical Engineering v 2648 1995. Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, USA. p 756-760
Publication Year: 1995
CODEN: PSISDG ISSN: 0277-786X ISBN: 0-8194-2021-2
Language: English

...Abstract: 1 at 80 K. The arrays were interconnected to silicon direct injection readout devices with **CCD** multiplexers which consist of input **circuits** , shift register and output **circuits** . The dynamical range was estimated to be of the order of 60 dB at T equals 80 K. The two- **phase** p-channel **CCD** **shift** register was designed with clock frequency operation less than or equal to 5 MHz. Transfer...
Descriptors: Infrared devices; Semiconducting cadmium compounds; **Semiconductor** diodes; Photolithography; Multiplexing; Charge coupled devices; Signal processing; **Analog** to **digital** conversion; Single crystals; Indium

20/3,K/8 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02334248 JICST ACCESSION NUMBER: 95A0607340 FILE SEGMENT: JICST-E
Phase-Unwrapping Hybrid System for High Speed Fringe Analysis Using CCD **Driving Clock Pulse.**
ARAI YASUHIKO (1); YAMADA TOMOHARU (1); YOKOZEKI SHUNSUKE (2)
(1) Kansai Univ., Fac. of Eng.; (2) Kyushu Inst. of Technol., Comput. Sci. and Syst. Eng.
Kogaku(Japanese Journal of Optics), 1995, VOL.24,NO.7, PAGE.440-444, FIG.10, TBL.1, REF.8
JOURNAL NUMBER: G0125BAD ISSN NO: 0389-6625
UNIVERSAL DECIMAL CLASSIFICATION: 681.3:621.397.3 535.41.08:681.787
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

Phase-Unwrapping Hybrid System for High Speed Fringe Analysis Using CCD **Driving Clock Pulse.**
...ABSTRACT: utilizes a relative phase difference between the driving pulses and the vedio signal of a **CCD** . Experimental results show that the new hybrid system can perform a high speed fringe analysis...
...measuring system is estimated as close to that of the FFT method by using a **digital** computer. (author abst.)
...DESCRIPTORS: **phase** **shift** ; ...

... **analog** system...

... **circuit** ; ...

... **CCD** camera
...BROADER DESCRIPTORS: **semiconductor** device...

... **solid** **state** device...

... **image** **pickup** apparatus

File 344:Chinese Patents Abs Aug 1985-2004/May
(c) 2004 European Patent Office
File 347:JAPIO Nov 1976-2004/Apr(Updated 040802)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200456
(c) 2004 Thomson Derwent

Set	Items	Description
S1	116284	(SEMICONDUCTOR?? OR SEMI()CONDUCTOR??? OR SOLID()STATE?? OR SOLIDSTATE?? OR IC OR CHIP?? OR CIRCUIT??) AND (IMAGE??(2N)S-ENS??? OR CCD OR IMAGE()PICK??? OR PHOTOCELL?? OR PHOTODETECT-OR?? OR PHOTOSENSOR??)
S2	13569	ANALOG(2N)(CIRCUIT?? OR IC OR CHIP??)
S3	36573	DIGITAL(2N)(CIRCUIT?? OR IC OR CHIP??)
S4	54367	PHASE(5N)SHIFT???
S5	516	(S2 AND S3) AND CLOCK??
S6	97803	NOISE??(2N)(REDUC???? OR MINIMIZ??? OR SUPPRESS???)
S7	263	AU=(KOYAMA E? OR KOYAMA, E?)
S8	203	S1 AND S2 AND S3
S9	1	S8 AND S4
S10	15	S1 AND ANALOG?? AND DIGITAL?? AND S4
S11	3	S10 AND CLOCK?
S12	0	S11 AND S6
S13	9	S7 AND S1
S14	1	S13 AND S4
S15	8	S13 NOT S14
S16	0	S15 AND (S3 AND S2)

9/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04561416 **Image available**
IMAGE PICKUP DEVICE WITH FRAME STILL PICTURE GENERATING FUNCTION

PUB. NO.: 06-233316 [JP 6233316 A]
PUBLISHED: August 19, 1994 (19940819)
INVENTOR(s): SAKAGUCHI TAKASHI
KUSAKA HIROYA
NAKAYAMA MASAAKI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-015171 [JP 9315171]
FILED: February 02, 1993 (19930202)
JOURNAL: Section: E, Section No. 1633, Vol. 18, No. 608, Pg. 142, November 18, 1994 (19941118)

IMAGE PICKUP DEVICE WITH FRAME STILL PICTURE GENERATING FUNCTION

ABSTRACT

...by changing the vertical phases of three chrominance signals through the 1st and 2nd vertical **phase shift** parts and carrying out the still picture generation processing with use of a pseudo frame signal generated by a frame computing **circuit** .

...

...CONSTITUTION: The R, G and B output signals transmitted from an **image pickup** element part 101 are turned into the digital signals by an A/D converter 105 via an **analog** signal processing **circuit** 104 and then supplied to a **digital** signal processing **circuit** 106. The **circuit** 106 includes the Y(sub 1) and Y(sub 2) matrix **circuits** which generate the luminance signals Y(sub 1) and Y(sub 2) and the C(sub 1) and C(sub 2) matrix **circuits** which generate the chrominance signals C(sub 1) and C(sub 2) respectively. Then the **circuit** 106 applies the aperture processing, the coring processing, etc., to the signals Y(sub 1...

... 1) and C(sub 2) respectively. These processed signals are supplied to a field memory **circuit** 107 and a frame still picture is obtained by a field memory control **circuit** 108 based on those signals supplied to the **circuit** 107.

11/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06809252 **Image available**
IMAGE READER AND IMAGE PROCESSOR PROVIDED WITH THE IMAGE READER

PUB. NO.: 2001-036738 [JP 2001036738 A]
PUBLISHED: February 09, 2001 (20010209)
INVENTOR(s): NAGASE MASASHIRO
APPLICANT(s): RICOH CO LTD
APPL. NO.: 11-202182 [JP 99202182]
FILED: July 15, 1999 (19990715)

ABSTRACT

... the influence of a noise component to be superposed at the time of executing an **analog** composition of odd and even number pixels at a high speed in image reading by a **CCD** and adjusting an image signal level to secure linearity even in an intermediate gradation area...

...odd and even number pixel signals of a white reference board read out by a **CCD** 32 are processed at fixed gain by an **analog** processing **circuit** 50 and the composite signal is A/D-converted by A/D conversion **circuits** 44 respectively prepared for odd and even number pixels. After the conversion, an odd-even difference detection **circuit** 48 outputs a phase control instruction to a phase control **circuit** 49 in accordance with an odd-even difference calculated from the white reference board reading data stared in a **digital** value detection register 47 and the odd-even difference is corrected by repeating operation for **shifting** the **phase** of a sampling **clock** of the A/D conversion **circuits** 44 unitl the odd-even difference is included in a target value.

11/3,K/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06722014 **Image available**
IMAGE READER

PUB. NO.: 2000-307852 [JP 2000307852 A]
PUBLISHED: November 02, 2000 (20001102)
INVENTOR(s): TAGUCHI KAZUE
APPLICANT(s): RICOH CO LTD
APPL. NO.: 11-112504 [JP 99112504]
FILED: April 20, 1999 (19990420)

ABSTRACT
... TO BE SOLVED: To provide an image reader which adjusts the input timing of a **clock** highly accurately without changing hardware, in the case of changing **image sensors** and the input timing of a drive (sampling) **clock** in an ADC that performs A/D conversion of its image output.

SOLUTION: The phase of a driver **clock** is adjusted by setting adjustment data from a CPU 101 to the register of a timing **circuit** 112, which outputs an ADCLK for sampling to ADCs (R, G and B) 119 to 121, outputs an ICLK and a three-line **CCD** 111 to an image processing system and outputs a drive **clock** to an **analog** processing system, etc. White reference is used in an adjustment operation mode, a **digital** value detection **circuit** 122 is served also as a shading correction **circuit** and a memory detects outputs of the ADCs 119 to 121 of each **phase** obtained, by **shifting** an image **clock** by a reciprocal of the integral multiples, and the input timing of the **clock** is adjusted by evaluating the value, selecting an optimum phase and setting it as adjustment...

11/3,K/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008697837 **Image available**
WPI Acc No: 1991-201857/199128
XRPX Acc No: N91-154401
Optical fibre Sagnac interferometer - has digital **phase ramp resetting and is used for measuring low rotation rates**
Patent Assignee: LITEF GMBH (LITE-N); GROLLMANN P (GROL-I)
Inventor: GROELLMANN P
Number of Countries: 009 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 436052	A	19910710	EP 90100103	A	19900103	199128	B
CA 2026961	A	19910704				199137	
US 5116127	A	19920526	US 90633420	A	19901224	199224	
EP 436052	B1	19920923	EP 90100103	A	19900103	199239	
DE 59000320	G	19921029	DE 500320	A	19900103	199245	
			EP 90100103	A	19900103		
CA 2026961	C	19951121	CA 2026961	A	19901004	199607	

Priority Applications (No Type Date): EP 90100103 A 19900103
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 436052	A				
Designated States (Regional): DE ES FR GB IT NL SE					
US 5116127	A		16	G01C-019/72	
EP 436052	B1	G	20	G01C-019/72	
Designated States (Regional): DE ES FR GB IT NL SE					
DE 59000320	G			G01C-019/72	Based on patent EP 436052
CA 2026961	C			G01C-019/72	

... **has** digital **phase ramp resetting and is used for measuring low rotation rates**

...Abstract (Basic): The interferometer has a **digital** regulating **circuit** for phase ramp resetting, with a scale factor correction **circuit** used for demodulation of the amplified **photodetector** output signals (VD); in synchronism with the mode switching, an integration amplifier (1A) used to provide an **analogue** scale factor correction signal (SIA ...

...The synchronous demodulator (SYNCD1) for the **photodetector** signals (VD') is coupled via an A/D converter (AD) to a **digital** integrator (M1, ADD1, M2), with a **digital** adder (ADD2) between the latter and a DIA converter (DA) providing a feedback signal (VC...
...Abstract (Equivalent): between two operating modes (A, B) in time with the frequency f0 a reciprocal alternating **phase** **shift** (Om) of the two counter-rotating light beams, and - a second signal component being a...

...transit time t0 or integral multiples of t0, and amplitude increments which compensate nonreciprocal incremental **phase** **shifts** of the two light beams, - the amplified **photodetector** output signal (VD') is fed to a first synchronous demodulator (SYNCD1) **clocked** with the frequency f0, - the demodulated and amplified output signal (VA) is fed to an **analog** -to- **digital** converter (AD) and after digitisation integrated in a **digital** integrator (M1, ADD1, M2) and is applied to the phase modulator (AM) via a **digital** -to- **analog** converter (DA) and a driver amplifier (AP), in order to compensate nonreciprocal **phase shifts** of the light beams by means of the second signal component, - a scale factor correction **circuit** is provided which demodulates the amplified **photodetector** output signal (VD') in time with the mode reversal and transmits an **analog** scale factor correction signal (SIA) to the **digital** -to- **analog** converter (DA) via an integrating amplifier (IA), and in which - a processor (CPU) supplies the control and synchronisation signals for the first synchronous demodulator (SYNCD1), the **analog** -to- **digital** converter (AD) and the **digital** integrator (M1, ADD1, M2) wherein - between the **digital** integrator (M1, ADD1, M2) and the **digital** -to- **analog** converter (DA) there is arranged a **digital** adder (ADD2) to which at a second input the modulation deviation signal that can be...

...operating modes (A or B) is applied from a first pulse generator (GEN1) that is **clocked** with the frequency f0 and is set up to transmit to the second input of the **digital** adder (ADD2) a signal corresponding to the phase deviation + pi/4 for the first operating...

...Abstract (Equivalent): The fibre optic sagnac interferometer rotation rate sensor is reset by phase ramp via a **digital** control **circuit** to undertake the reversal required to obtain the scale factor error information, a reciprocal, alternating **phase** **shift** that is not a function of the angle of rotation, but has a fixed timing...

...Title Terms: **DIGITAL** ;

14/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014678112
WPI Acc No: 2002-499169/200253
XRPX Acc No: N02-395169

Semiconductor **integrated** circuit **e.g. CMOS type** solid - state image sensing **device has selection** circuit **that selects only** phase shift circuit **providing noise component of minimum value**

Patent Assignee: SHARP KK (SHAF); KOYAMA E (KOYA-I)
Inventor: **KOYAMA E**
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020047632	A1	20020425	US 2001883990	A	20010620	200253	B
JP 2002009243	A	20020111	JP 2000184736	A	20000620	200253	
KR 2002000495	A	20020105	KR 200135042	A	20010620	200253	
KR 404677	B	20031107	KR 200135042	A	20010620	200418	

Priority Applications (No Type Date): JP 2000184736 A 20000620
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020047632	A1		13	H05B-037/02	
JP 2002009243	A		9	H01L-027/04	
KR 2002000495	A			H03L-007/00	
KR 404677	B			H03L-007/00	Previous Publ. patent KR 2002000495

Semiconductor **integrated** circuit **e.g. CMOS type** solid - state image sensing **device has selection** circuit **that selects only** phase shift circuit **providing noise component of minimum value**
Inventor: **KOYAMA E**

Abstract (Basic):

... A noise measuring **circuit** measures a noise component generated by an analog **circuit** , when **phase shift circuits** (16-18) are selected successively. A selection **circuit** (26) selects **phase shift circuit** that provides noise component of minimum value, based on output of a comparator (25) that...

... E.g. CMOS type **solid - state image sensing** device...

...Noise component generated by analog **circuit** is minimized, even when variation in transistor characteristics or resistance occurs in **semiconductor** integrated **circuits** in the manufacturing stage...

Title Terms: **SEMICONDUCTOR ;**

```
File   9:Business & Industry(R) Jul/1994-2004/Sep 01
         (c) 2004  The Gale Group
File  15:ABI/Inform(R) 1971-2004/Sep 02
         (c) 2004 ProQuest Info&Learning
File  16:Gale Group PROMT(R) 1990-2004/Sep 02
         (c) 2004 The Gale Group
File  20:Dialog Global Reporter 1997-2004/Sep 02
         (c) 2004 The Dialog Corp.
File  47:Gale Group Magazine DB(TM) 1959-2004/Sep 02
         (c) 2004 The Gale group
File  75:TGG Management Contents(R) 86-2004/Aug W4
         (c) 2004 The Gale Group
File  80:TGG Aerospace/Def.Mkts(R) 1986-2004/Sep 02
         (c) 2004 The Gale Group
File  88:Gale Group Business A.R.T.S. 1976-2004/Sep 01
         (c) 2004 The Gale Group
File  98:General Sci Abs/Full-Text 1984-2004/Jul
         (c) 2004 The HW Wilson Co.
File 112:UBM Industry News 1998-2004/Jan 27
         (c) 2004 United Business Media
File 141:Readers Guide 1983-2004/Jul
         (c) 2004 The HW Wilson Co
File 148:Gale Group Trade & Industry DB 1976-2004/Sep 02
         (c)2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2004/Sep 02
         (c) 2004 The Gale Group
File 264:DIALOG Defense Newsletters 1989-2004/Sep 02
         (c) 2004 The Dialog Corp.
File 484:Periodical Abs Plustext 1986-2004/Aug W4
         (c) 2004 ProQuest
File 553:Wilson Bus. Abs. FullText 1982-2004/Jul
         (c) 2004 The HW Wilson Co
File 570:Gale Group MARS(R) 1984-2004/Sep 02
         (c) 2004 The Gale Group
File 608:KR/T Bus.News. 1992-2004/Sep 02
         (c)2004 Knight Ridder/Tribune Bus News
File 620:EIU:Viewswire 2004/Sep 01
         (c) 2004 Economist Intelligence Unit
File 613:PR Newswire 1999-2004/Sep 02
         (c) 2004 PR Newswire Association Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Sep 02
         (c) 2004 The Gale Group
File 623:Business Week 1985-2004/Sep 01
         (c) 2004 The McGraw-Hill Companies Inc
File 624:McGraw-Hill Publications 1985-2004/Sep 01
         (c) 2004 McGraw-Hill Co. Inc
File 634:San Jose Mercury  Jun 1985-2004/Sep 01
         (c) 2004 San Jose Mercury News
File 635:Business Dateline(R) 1985-2004/Sep 02
         (c) 2004 ProQuest Info&Learning
File 636:Gale Group Newsletter DB(TM) 1987-2004/Sep 02
         (c) 2004 The Gale Group
File 647:CMP  Computer Fulltext 1988-2004/Aug W4
         (c) 2004 CMP Media, LLC
File 696:DIALOG Telecom. Newsletters 1995-2004/Sep 01
         (c) 2004 The Dialog Corp.
File 674:Computer News Fulltext 1989-2004/Aug W3
         (c) 2004 IDG Communications
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File 810:Business Wire 1986-1999/Feb 28
(c) 1999 Business Wire
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc
File 587:Jane`s Defense&Aerospace 2004/Aug W3
(c) 2004 Jane`s Information Group

Set	Items	Description
S1	15824	(SEMICONDUCTOR?? OR SEMI()CONDUCTOR??? OR SOLID()STATE?? OR SOLIDSTATE?? OR IC OR CHIP?? OR CIRCUIT??)(S)(IMAGE??(2N)SENS??? OR CCD OR IMAGE()PICK??? OR PHOTOCELL?? OR PHOTODETECTOR-?? OR PHOTOSENSOR??)
S2	44036	ANALOG(2N)(CIRCUIT?? OR IC OR CHIP??)
S3	67928	DIGITAL(2N)(CIRCUIT?? OR IC OR CHIP??)
S4	19626	PHASE(5N)SHIFT???
S5	252	(S2(S)S3)(S)CLOCK??
S6	73799	NOISE??(2N)(REDUC???? OR MINIMIZ??? OR SUPPRESS???)
S7	22	AU=(KOYAMA E? OR KOYAMA, E?)
S8	0	S7 AND S1
S9	0	S7 AND S2
S10	0	S7 AND S3
S11	307	S1(S)S2
S12	71	S11(S)S3
S13	0	S12(S)S4
S14	283	S4(5N)CLOCK?
S15	0	S12(S)S14
S16	6	ANALOG?(S)DIGITAL?(S)S14
S17	5	RD (unique items)
S18	0	S17 AND S1
S19	345647	ANALOG?(S)DIGITAL?
S20	1001	S1(S)S19
S21	0	S20 AND S14
S22	32	S19 AND S14
S23	0	S22 AND S1

17/3,K/1 (Item 1 from file: 9)
DIALOG(R)File 9:Business & Industry(R)

2106485 Supplier Number: 02106485 (USE FORMAT 7 OR 9 FOR FULLTEXT)
Experiment bridges studio-monitoring, high-end consumer systems -- Sony tips its digital-speaker work
(Sony Electronics develops a speaker prototype that is a combination of state-of-the-art electronics and transducer technologies)
Electronic Engineering Times, p 100
April 06, 1998
DOCUMENT TYPE: Journal ISSN: 0192-1541 (United States)
LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 1036

(USE FORMAT 7 OR 9 FOR FULLTEXT)

TEXT:
...times more powerful than the 24-bit Motorola 56000 processor. Six are used in the **digital** speaker system, to maintain the equivalent 24-bit performance on data sampled at 96 kHz...

...said Anagnos. "This would require hundreds of thousands of taps if we did this with **analog** circuitry." The DSP speaker architecture uses separate left data, right data and **clock** signals to keep jitter and **phase shifts** at a minimum. The goal is to keep noise, distortion and **digital** artifacts below the level of 24-bit A/D and D/A converters.

Speaker makers...

17/3,K/2 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

05546213 Supplier Number: 48406781 (USE FORMAT 7 FOR FULLTEXT)
Experiment bridges studio-monitoring, high-end consumer systems: Sony tips its digital-speaker work
Ohr, Stephan
Electronic Engineering Times, p100
April 6, 1998
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1056

... times more powerful than the 24-bit Motorola 56000 processor. Six are used in the **digital** speaker system, to maintain the equivalent 24-bit performance on data sampled at 96 kHz...

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Speaker makers...

17/3,K/3 (Item 1 from file: 148)

DIALOG(R)File 148:Gale Group Trade & Industry DB

11589886 SUPPLIER NUMBER: 55897012 (USE FORMAT 7 OR 9 FOR FULL TEXT)
New Architectures, ICs, Processes To Open Communication Frontiers.
GOLDBERG, LEE
Electronic Design, 45, 9, 68
May 1, 1997
ISSN: 0013-4872 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1876 LINE COUNT: 00158

... on-chip PLLs bypasses the costly and difficult task of implementing a few highly demanding **analog** functions on a predominantly **digital** chip.

17/3,K/4 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02070918 SUPPLIER NUMBER: 19426718 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Acquisition clock dithering in a digital oscilloscope. (Technology Information)(Technical)
Toeppen, Derek E.
Hewlett-Packard Journal, v48, n2, p26(3)
April, 1997
DOCUMENT TYPE: Technical ISSN: 0018-1153 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1698 LINE COUNT: 00133

... in Fig. 4. In this circuit, the error voltage is generated by a 8-bit **digital** -to-analog converter (DAC). This provides (2.sup.8) or 256 discrete **phase shifts** in the acquisition **clock** . The 8-bit **digital** word written to the DAC is pseudorandomly generated by one of the oscilloscope's processors...

17/3,K/5 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01157772 CMP ACCESSION NUMBER: EET19980406S0146
Experiment bridges studio-monitoring, high-end consumer systems - Sony tips its digital-speaker work
Stephan Ohr
ELECTRONIC ENGINEERING TIMES, 1998, n 1001, PG100
PUBLICATION DATE: 980406
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: News Feature
WORD COUNT: 1049

... times more powerful than the 24-bit Motorola 56000 processor. Six are used in the **digital** speaker system, to maintain the equivalent 24-bit performance on data sampled at 96 kHz...

...said Anagnos. "This would require hundreds of thousands of taps if we did this with **analog** circuitry." The DSP speaker architecture uses

separate left data, right data and **clock** signals to keep jitter and **phase shifts** at a minimum. The goal is to keep noise, distortion and **digital** artifacts below the level of 24-bit A/D and D/A converters.

Speaker makers...

```
File 348:EUROPEAN PATENTS 1978-2004/Aug W04
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040826,UT=20040819
         (c) 2004 WIPO/Univentio

Set     Items   Description
S1      21138    (SEMICONDUCTOR?? OR SEMI()CONDUCTOR??? OR SOLID()STATE?? OR
               SOLIDSTATE?? OR IC OR CHIP?? OR CIRCUIT??)(S)(IMAGE??(2N)SEN-
              S??? OR CCD OR IMAGE()PICK??? OR PHOTOCELL?? OR PHOTODETECTOR-
              ?? OR PHOTOSENSOR??)
S2      15943   ANALOG(2N)(CIRCUIT?? OR IC OR CHIP??)
S3      25475   DIGITAL(2N)(CIRCUIT?? OR IC OR CHIP??)
S4      33040   PHASE(5N)SHIFT???
S5        789   (S2(S)S3)(S)CLOCK??
S6      33083   NOISE??(2N)(REDUC???? OR MINIMIZ??? OR SUPPRESS???)
S7         15   AU=(KOYAMA E? OR KOYAMA, E?)
S8          1   S7 AND S1
S9          0   S7 AND S2 AND S3
S10       673   S1(S)S2
S11       246   S10(S)S3
S12         3   S11(S)S4
S13         0   S12(S)CLOCK?
S14      2608   S1(S)ANALOG???(S)DIGITAL??
S15        24   S14(S)S4
S16         9   S15(S)CLOCK?
S17         9   S16 NOT (S12 OR S8)
S18         1   S17(S)S6
S19       113   S1 AND S2 AND S3 AND S4
S20      1477   S4(5N)CLOCK?
S21         8   S19 AND S20
S22         0   S21 AND S6
S23         7   S21 NOT (S16 OR S8 OR S18)
```

8/5,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00545774
Solid state image pickup **apparatus having microlenses**
Festkorperbildaufnahmevorrichtung mit Mikrolinsen
Capteur d'image a l'etat solide ayant des microlentilles
PATENT ASSIGNEE:
SHARP KABUSHIKI KAISHA, (260710), 22-22 Nagaike-cho Abeno-ku, Osaka 545, (JP), (applicant designated states: DE;FR;GB;NL)
INVENTOR:
Koyama, Eiji , 2613-1, Ichinomoto-cho, Tenri-shi, Nara-ken, (JP
LEGAL REPRESENTATIVE:
Brown, Kenneth Richard et al (28831), R.G.C. Jenkins & Co. 26 Caxton Street, London SW1H 0RJ, (GB)
PATENT (CC, No, Kind, Date): EP 542581 A1 930519 (Basic)
EP 542581 B1 960717
APPLICATION (CC, No, Date): EP 92310454 921116;
PRIORITY (CC, No, Date): JP 91300668 911115
DESIGNATED STATES: DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: H01L-031/0232; H01L-031/0216;
CITED PATENTS (EP A): EP 444212 A; EP 441594 A; US 4667092 A; EP 242663 A
CITED REFERENCES (EP A):
IEEE TRANSACTIONS ON CONSUMER ELECTRONICS vol. 37, no. 3, August 1991, NEW YORK US pages 487 - 492 SAKAKIBARA ET AL. 'A 1" FORMAT 1.5M PIXEL IT-CCD IMAGE SENSOR FOR AN HDTV CAMERA';

ABSTRACT EP 542581 A1
Solid image pickup apparatus, wherein a light screening film (9) is formed with the conventional art, a polyamide resin (10a) which is a transparent resin larger in refractive index than the microlens (11) material is applied by a spin coating method, then, it is baked for 5 through 10 minutes at 200(degree) through 250(degree)C so as to form a flattened film 10a, thereafter, an acrylic resin is coated by a spin coating method. (see image in original document)
ABSTRACT WORD COUNT: 80

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	930519	A1	Published application (Alwith Search Report ;A2without Search Report)
Examination:	930915	A1	Date of filing of request for examination: 930721
Examination:	941109	A1	Date of despatch of first examination report: 940923
Grant:	960717	B1	Granted patent
Oppn None:	970709	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPAB96	158
CLAIMS B	(German)	EPAB96	129
CLAIMS B	(French)	EPAB96	183
SPEC B	(English)	EPAB96	1855
Total word count - document A			0
Total word count - document B			2325
Total word count - documents A + B			2325

Solid state image pickup **apparatus having microlenses**

INVENTOR:
Koyama, Eiji ...

...SPECIFICATION B1

BACKGROUND OF THE INVENTION

The present invention generally relates to a **solid - state image pickup** apparatus having a microlens.

A structural sectional view of the conventional **solid - state image pickup** apparatus will be described with reference to Fig. 3. A light receiving portion 3 and...

...provided on the surface portion of a P well region 2 on an N type **semiconductor** basic plate 1 as shown in Fig. 3. A silicon oxide film 5 is deposited...

...denotes an optical system lens, reference numeral 13 an iris, and reference numeral 14 a **solid - state image pickup** apparatus.

A **solid - state image pickup** apparatus 14 is positioned, as shown in Fig. 4, in a location where light is...

...THE INVENTION

In one aspect the present invention, as defined by claim 1, provides a **solid - state image pickup** device comprising an array of photosensitive elements formed in a **semiconductor** structure, a flattening film formed over said **semiconductor** structure, and an array of microlenses formed over said flattening film, wherein the refractive index...

...the flattening film is larger than that of the microlenses.

According to the invention the **solid - state image pickup** device is improved in its light-collection efficiency since, as shown in Fig. 6, light...

...aspect the present invention, as defined by claim 3, provides a processing for manufacturing this **solid - state image pickup** device.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a structural sectional view of one...

...embodiment of the present invention;

Fig. 3 is a structural sectional view of a conventional **solid - state image pickup** apparatus;

Fig. 4 is a sectional view of an optical system mechanism such as a camera;

Fig. 5 is an incident light passage view of the conventional **solid - state image pickup** apparatus in a mechanism shown in Fig. 4;

Fig. 6 is an incident light passage...

...CLAIMS B1

1. A **solid - state image pickup** device comprising an array of photosensitive elements (3) formed in a **semiconductor** structure (1 to 9), a flattening film (10a) formed over said **semiconductor** structure, and an array of microlenses formed over said flattening film, characterized in that the refractive index of the flattening film is larger than that of the microlenses.

2. A **solid - state image pickup** device according to claim 1, wherein said flattening film (10a) comprises polyamide resin and said microlenses (11) comprise acrylic resin.
3. A process of manufacturing the **solid - state image pickup** device defined by claim 2, comprising:
forming said semiconductor structure having said array of photosensitive...

12/5,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01266170
FLUOROGENIC COMPOUNDS AND USES THEREFOR
FLUOROGENE VERBINDUNGEN UND IHRE VERWENDUNGEN
COMPOSES FLUOROGENES ET LEURS UTILISATIONS
PATENT ASSIGNEE:
  3M Innovative Properties Company, (2739383), 3M Center, P.O. Box 33427,
    Saint Paul, MN 55133-3427, (US), (Proprietor designated states: all)
INVENTOR:
  BENTSEN, James, G., Post Office Box 33427, Saint Paul, MN 55133-3427,
    (US)
  MICKLESON, Christopher, A., Post Office Box 33427, Saint Paul, MN
    55133-3427, (US)
  KNUDSON, Orlin, B., Post Office Box 33427, Saint Paul, MN 55133-3427,
    (US)
  LEWANDOWSKI, Kevin, M., Post Office Box 33427, Saint Paul, MN 55133-3427,
    (US)
LEGAL REPRESENTATIVE:
  VOSSIUS & PARTNER (100314), Siebertstrasse 4, 81675 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1204671 A1 020515 (Basic)
                             EP 1204671 B1 031203
                             WO 2001010881 010215
APPLICATION (CC, No, Date): EP 2000953743 000728; WO 2000US20715 000728
PRIORITY (CC, No, Date): US 147307 P 990805; US 611686 000707
DESIGNATED STATES (Pub A): AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE;
  IT; LI; LU; MC; NL; PT; SE; (Pub B): DE; ES; FR; GB; IT; SE
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: C07H-017/075; C07D-409/04; C07D-407/04;
  C12Q-001/22; G01N-033/58
CITED PATENTS (EP B): EP 223162 A; EP 645382 A; US 4259233 A; US 5236827 A;
  US 5418167 A
CITED PATENTS (WO A): EP 223162 A ; EP 645382 A ; US 5418167 A ; US 4259233
  A ; US 5236827 A
ABSTRACT WORD COUNT: 24911
NOTE:
  No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	010411	A1	International application. (Art. 158(1))
Application:	010411	A1	International application entering European phase
Application:	020515	A1	Published application with search report
Examination:	020515	A1	Date of request for examination: 20020227
Examination:	020814	A1	Date of dispatch of the first examination report: 20020701
Grant:	031203	B1	Granted patent
Lapse:	040609	B1	Date of lapse of European Patent in a contracting state (Country, date): SE 20040303,

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200349	1514
CLAIMS B	(German)	200349	1445
CLAIMS B	(French)	200349	1889
SPEC B	(English)	200349	21764
Total word count - document A			0

Total word count - document B   26612
Total word count - documents A + B   26612

...SPECIFICATION diodes can be sine-wave modulated or pulsed and used in conjunction with the red- **shifted** FESs of the present invention **to** offer advantages for multiplexing and signal-to-noise discrimination. Diode laser and light emitting diode...

...auto-fluorescence can occur or wavelengths that overlap the excitation wavelength band centered at (lambda) **1**)) where background signals from scattered excitation light can interfere. The filtered fluorescent return signal is...

12/5,K/2   (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00615569
IMAGING DEVICE WITH HORIZONTAL LINE INTERPOLATION FUNCTION
BILDAUFNAHMEVORRICHTUNG MIT INTERPOLATIONSFUNKTION DER HORIZONTALEN ZEILEN
DISPOSITIF D'IMAGERIE A FONCTION D'INTERPOLATION DES LIGNES HORIZONTALES
PATENT ASSIGNEE:
  MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., (216883), 1006, Oaza Kadoma, Kadoma-shi, Osaka-fu, 571, (JP), (Proprietor designated states: all)
INVENTOR:
  KUSAKA, Hiroya, 1-5-3, Terahata, Kawanishi-shi, Hyogo 666, (JP)
  SAKAGUCHI, Takashi, 8-11-309, Syowa-cho, Yamatotakada-shi, Nara 635, (JP)
  NAKAYAMA, Masaaki, 2-44-8, Higashihunahashi, Hirakata-shi, Osaka 573, (JP)
LEGAL REPRESENTATIVE:
  Rackham, Stephen Neil et al (35061), GILL JENNINGS & EVERY, Broadgate House, 7 Eldon Street, London EC2M 7LH, (GB)
PATENT (CC, No, Kind, Date): EP 605738 A1 940713 (Basic)
                              EP 605738 A1 950215
                              EP 605738 B1 000223
                              WO 9403015 940203
APPLICATION (CC, No, Date):   EP 93916186 930719; WO 93JP1002 930719
PRIORITY (CC, No, Date): JP 92195095 920722; JP 92195096 920722; JP 92195097 920722; JP 92195099 920722; JP 9315171 930202
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H04N-009/09; H04N-009/04
CITED PATENTS (EP B): EP 477884 A; JP 55130284 A; JP 59160390 A; JP 2061248 B; JP 56054115 B; US 3975760 A

ABSTRACT EP 605738 A1
    The phases of three color signals in the vertical direction sent from a plurality of solid-state imaging elements arranged in the captioned device are shifted from each other. Thus, when the horizontal line interpolations are generated, it is possible to reduce the degradation of the frequency response characteristic in the vertical direction and of the sharpness of the image in the vertical direction when the interpolated video signals are viewed as the whole of the three color signals (for example, when a luminance signal generated by combining the G, R, B signals by a matrix operations is considered). Also, by generating pseudo frame signals, it is possible to produce a high quality stationary frame. (see image in original document)
ABSTRACT WORD COUNT: 121

LEGAL STATUS (Type, Pub Date, Kind, Text):

Oppn None:	010207 B1	No opposition filed: 20001124
Grant:	20000223 B1	Granted patent
Application:	940511 A	International application (Art. 158(1))
Application:	940713 A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	940713 A1	Date of filing of request for examination: 940419
Change:	950201 A1	Obligatory supplementary classification (change)
Search Report:	950215 A1	Drawing up of a supplementary European search report: 941223
Examination:	971217 A1	Date of despatch of first examination report: 971103

LANGUAGE (Publication,Procedural,Application): English; English; Japanese

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200008	1889
CLAIMS B	(German)	200008	1433
CLAIMS B	(French)	200008	2183
SPEC B	(English)	200008	17167
Total word count - document A			0
Total word count - document B			22672
Total word count - documents A + B			22672

...SPECIFICATION signal, and the solid state image pickup element 3 obtains a B signal. A vertical **phase shift** section 4 is included in the figure for schematically showing implementation of **phase shift** of a chrominance signal (where 2 and 4 are combined to form an image pickup section 6), and a vertical **phase shift** section 5 is included for schematically showing implementation of **phase shift** of a chrominance signal (where 3 and 5are combined to form an image pickup section obtained by the solid state image pickup elements 1, 2, 3; analog-to- **digital** converter **circuits** 11, 12, 13 are **circuits** for converting the three chrominance signals processed by the **analog** signal processing **circuits** 8, 9, 10, respectively, from analog to digital form; and an interpolation **circuit** 14 is a **circuit** for performing interpolation on the three chrominance signals converted to digital form by the analog-to- **digital** converter **circuits** 11, 12, 13. A matrix **circuit** 16 is a **circuit** for performing matrix operation on the three chrominance signals interpolated by the interpolation **circuit** 14 to synthesize a luminance signal and two color-difference signals, and an encoder **circuit** 17 is a **circuit** for obtaining an NTSC signal from the luminance and color-difference signals obtained by the matrix **circuit** 16. An **image pickup** element drive **circuit** 17 is a **circuit** for driving the **solid state image pickup** element 1. A system control **circuit** 19 is a **circuit** for comprehensively controlling the vertical **phase shift** sections 4, 5, and the interpolation **circuit** 14, and the **image pickup** element drive **circuit** 18.

FIG. 2 (a) shows an operation of the vertical phase shift sections 4, 5 ...

...8, 9, 10, respectively, then converted from analog to digital signals by the analog-to- **digital** converter **circuits** 11, 12, 13, and transmitted to the interpolation **circuit** 14. The G, R, and B signals transmitted to the interpolation **circuit** 14 are subjected to the respective interpolation processing, and this interpolation processing is here explained...

...to FIG. 4 (a) through FIG. 4 (d). First considered is the case where the **solid state image pickup** elements 2, 3 are shifted with respect to the **solid state image pickup** element 1 downward thereof (i.e. in the direction in which line number increases). When...

...and p1-w from the kth line of the R signal, taking into consideration the **phase shift** with respect to the G signal. This is the same also with the B signal...

...from the kth line of the B signal (FIG. 4 (a)), taking into consideration the **phase shift** with respect to the G signal. Meanwhile, if p1 ≤ w < 1, then the...

...w from the (k+1)th line of the R signal, taking into consideration the **phase shift** with respect to the G signal. This is the same also with the B signal...w from the (k+1)th line of the B signal, taking into consideration the **phase shift** with respect to the G signal (FIG. 4 (b)). Next considered is the case where the **solid state image pickup** elements 2, 3 are shifted with respect to the **solid state image pickup** element 1 upward (i.e. in the direction in which line number decreases). When a...

...w from the (k+1)th line of the R signal, taking into consideration the **phase shift** with respect to the G signal. This is the same also with the B signal...

...w from the (k+1)th line of the B signal, taking into consideration the **phase shift** with respect to the G signal (FIG. 4 (c)). Meanwhile, if p1 ≤ w <...

...w from the (k+2)th line of the R signal, taking into consideration the **phase shift** with respect to the G signal. This is the same also with the B signal...

...w from the (k+2)th line of the B signal, taking into consideration the **phase shift** with respect to the G signal (FIG. 4 (d)).

With an interpolation line synthesized in...second embodiment.

In the figure, solid state image pickup elements 31 and 32, a vertical **phase shift** section 34, analog signal processing circuits 38, 39, analog-to- **digital** converter **circuits** 41, 42, 43, an interpolation **circuit** 44, a matrix **circuit** 46, an encoder **circuit** 47, an **image pickup** element drive **circuit** 48, and a system control **circuit** 49 are respectively those which exhibit the same functions as the **solid state image pickup** elements 1, 2, the vertical **phase shift** section 4, the **analog** signal processing **circuits** 8, 9, the analog-to- **digital** converter **circuits** 11, 12, 13, the interpolation **circuit** 14, the matrix **circuit** 16, the encoder **circuit** 17, the **image pickup** element drive **circuit** 18, and the system control **circuit** 19, respectively, of the first embodiment as shown in FIG. 1. Therefore, their detailed description...signal separation circuit, and thereafter converted from analog to digital signals by the analog-to- **digital** converter **circuits** 41, 42, and 43, and then transmitted to the interpolation **circuit** 44. The G, R, and B signals transmitted to the interpolation **circuit** 44 are subjected to their corresponding interpolation processing and this interpolation processing is described with...

...to FIG. 11 (a) through FIG. 11 (d). First discussed is a case where the **solid state image pickup** element 32 is shifted downward with respect to the **solid state image pickup** element 31 (i.e. in the direction in which line number increases). When a line...

...the kth line of the R signal and the B signal, taking into consideration the **phase shift** with respect to the G signal (FIG. 11 (a)). Meanwhile, if p3 ≤ w <...

...1)th line of the R signal and the B signal, taking into consideration the **phase shift** with respect to the G signal (FIG. 11 (b)). Next discussed is the case where the **solid state image pickup** element 32 is shifted upward with respect to the **solid state image pickup** element 31 (i.e. in the direction in which line number decreases). When a line...

...1)th line of the R signal and the B signal, taking into consideration the **phase shift** with respect to the G signal (FIG. 11 (c)). Meanwhile, if p3 ≤ w <...
...2)th line of the R signal and the B signal, taking into consideration the **phase shift** with respect to the G signal (FIG. 11 (d)).
With an interpolation line synthesized in...

12/5,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00248671
Motor rotation control apparatus.
Motorumdrehungszahl-Regelgerat.
Appareil de commande de la rotation d'un moteur.
PATENT ASSIGNEE:
SONY CORPORATION, (214021), 7-35 Kitashinagawa 6-Chome Shinagawa-ku, Tokyo 141, (JP), (applicant designated states: DE;FR;GB;NL)
INVENTOR:
Machida, Yukihiko c/o Patent Division, Sony Corporation 6-7-35 Kitashinagawa, Shinagawa-ku Tokyo 141, (JP)
Tomitaka, Tadafusa c/o Patent Division, Sony Corporation 6-7-35 Kitashinagawa, Shinagawa-ku Tokyo 141, (JP)
LEGAL REPRESENTATIVE:
Cotter, Ivan John et al (29661), D. YOUNG & CO. 10 Staple Inn, London WC1V 7RD, (GB)
PATENT (CC, No, Kind, Date): EP 249465 A1 871216 (Basic)
EP 249465 B1 920108
APPLICATION (CC, No, Date): EP 87305148 870610;
PRIORITY (CC, No, Date): JP 86134685 860610; JP 86134684 860610
DESIGNATED STATES: DE; FR; GB; NL
INTERNATIONAL PATENT CLASS: G05D-013/62;
CITED PATENTS (EP A): US 4254367 A; US 4197489 A; GB 2123584 A

ABSTRACT EP 249465 A1
A motor rotation control apparatus employs a comb filter circuit (10) to filter out a signal component and its higher harmonics. An error signal (DS) indicative of an error between actual and target conditions of rotation of the motor is applied to the comb filter circuit (10) after a direct current component thereof is removed. The filtered signal and the error signal are added in a circuit (90) which produces a control

signal used to control rotation of the motor (50). Predetermined successive portions (samples) of the error signal may each be divided into a first digital signal portion having a predetermined number of upper bits of data and a second digital signal portion having the remaining lower bits of data. The lower bits are delayed a predetermined time and added to the error signal to compensate for lower bits of data which may be ignored in a digital-to-analog converter, operable on a limited number of bits, to provide an analog control signal used to control rotation of the motor.

ABSTRACT WORD COUNT: 174

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	871216	A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	880720	A1	Date of filing of request for examination: 880517
Examination:	900808	A1	Date of despatch of first examination report: 900622
Grant:	920108	B1	Granted patent
Oppn None:	921230	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	2653
CLAIMS B	(German)	EPBBF1	797
CLAIMS B	(French)	EPBBF1	1082
SPEC B	(English)	EPBBF1	6076
Total word count - document A			0
Total word count - document B			10608
Total word count - documents A + B			10608

...SPECIFICATION forming circuit 170 which forms a part of the speed servo loop. The pulses PG **are** fed from the second head 163 to a phase **error** data forming circuit 180 which forms a part of the phase servo loop.

The speed...

17/5,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00643169
Image scanning device
Bildabtastgerat
Dispositif de balayage d'images
PATENT ASSIGNEE:
SHARP KABUSHIKI KAISHA, (260710), 22-22 Nagaike-cho, Abeno-ku, Osaka-shi, Osaka-fu 545-0013, (JP), (applicant designated states: DE;FR;GB)
INVENTOR:
Nagano, Fumikazu, 46-13 Izumihara-cho, Yamato-Koriyama-shi, Nara-ken, (JP)
LEGAL REPRESENTATIVE:
Muller, Frithjof E., Dipl.-Ing. et al (8661), Patentanwalte MULLER & HOFFMANN, Innere Wiener Strasse 17, 81667 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 622955 A2 941102 (Basic)
EP 622955 A3 950111
EP 622955 B1 990714
APPLICATION (CC, No, Date): EP 94106525 940426;
PRIORITY (CC, No, Date): JP 10139893 930427; JP 15374493 930624
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H04N-005/335; H04N-005/217; H04N-001/028;
ABSTRACT EP 622955 A2
An image scanning device comprises a light source for emitting a beam, a CCD circuit board having a CCD sensor, an optical unit for guiding the emitted beam from the light source to the CCD sensor, a CCD sensor driving circuit connected with the CCD circuit board with a signal cable, a clock generating circuit for generating a clock to be transferred to the CCD sensor, a reset pulse generating circuit for generating a reset pulse for resetting an output buffer of the CCD sensor, a clamp circuit for clamping an output of the CCD sensor, and an analog-to-digital converter for converting an analog signal into a digital signal. The clock generating circuit is disposed on the CCD circuit board. The reset pulse generating circuit is disposed on the CCD circuit board. The CCD sensor driving circuit comprises a fast clock generator for feeding clocks to a CCD element at fast speed and a voltage attenuator for attenuating a voltage of the fast clocks. The optical unit includes a light condensing means for condensing the beam emitted from the light source to a front point of the light source, the light source irradiating the beam on a manuscript surface. The image scanning device further comprises an actuating means for actuating the reset means and the clamp means one time for a plurality of outputs of the CCD sensor, a first latch means for latching an output of the analog-to-digital converter, a second latch means for latching for latching an output of the first latch means, and a subtracting means for subtracting the output of the second latch means from the output of the first latch means. (see image in original document)
ABSTRACT WORD COUNT: 284

LEGAL STATUS (Type, Pub Date, Kind, Text):

Oppn None:	000628 B1	No opposition filed: 20000415
Application:	941102 A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	950111 A3	Separate publication of the European or International search report
Examination:	950614 A2	Date of filing of request for examination: 950411

Change: 970319 A2 Representative (change)
Examination: 970514 A2 Date of despatch of first examination report: 970402
Change: 971217 A2 Representative (change)
Change: 980114 A2 Representative (change)
Grant: 990714 B1 Granted patent
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9928	396
CLAIMS B	(German)	9928	322
CLAIMS B	(French)	9928	454
SPEC B	(English)	9928	7969
Total word count - document A			0
Total word count - document B			9141
Total word count - documents A + B			9141

...CLAIMS emitted beam from said light source (13) to said CCD sensor (61; 20); and
an **analog** processing **circuit** (70) including a clamp **circuit** (71) for clamping an output of said **CCD** sensor (61; 20) and an **analog** -to- **digital** converter (72) for converting an **analog** output signal of said **CCD** sensor (61; 20) into a **digital** signal, characterized in that
- said **clock** generating **circuit** (62) and said reset pulse generating **circuit** (63) are disposed on said **CCD** **circuit** board (15) so as to drive said **CCD** sensor (61; 20) at high speed without causing a **phase** **shift** between the **clock** signals and radio wave noise on a signal line.
2. An image scanning device according...

17/5,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00412551
Fiber optic Sagnac interferometer with digital phase resetting for measuring rotation rate.
Faseroptisches Sagnac-Interferometer mit digitaler Phasenrampenruckstellung zur Drehratenmessung.
nnterferometre de Sagnac a fibre optique avec rappel numerique de dephasage pour la mesure de la vitesse de rotation.
PATENT ASSIGNEE:
LITEF GmbH, (508641), Lorracher Strasse 18, W-7800 Freiburg/Br., (DE), (applicant designated states: DE;ES;FR;GB;IT;NL;SE)
INVENTOR:
Grollmann, Peter, Dipl.-Ing., Feldbergstrasse 24L, W-7800 Freiburg i.Br., (DE)
LEGAL REPRESENTATIVE:
TER MEER - MULLER - STEINMEISTER & PARTNER (100061), Mauerkircherstrasse 45, W-8000 Munchen 80, (DE)
PATENT (CC, No, Kind, Date): EP 436052 A1 910710 (Basic)
EP 436052 B1 920923
APPLICATION (CC, No, Date): EP 90100103 900103;
PRIORITY (CC, No, Date): EP 90100103 900103
DESIGNATED STATES: DE; ES; FR; GB; IT; NL; SE
INTERNATIONAL PATENT CLASS: G01C-019/72;

CITED PATENTS (EP A): EP 168292 A; GB 2152207 A; EP 294915 A; EP 359666 A

ABSTRACT EP 436052 A1 (Translated)

To prevent a lock-in effect and to prevent scale factor nonlinearities, particularly at low rates of rotation, it is proposed for a fibre-optic interferometer-type rate-of-rotation sensor, the phase ramp of which is reset via a digital control loop, to carry out the switching-over of a reciprocal, alternating phase shift, required for obtaining the scale factor error information, not as a function of the angle of rotation but with a fixed timing which can be preferably synchronised with the gyroscope modulation frequency. The advantage of the invention is that, particularly also in the case of small rates of rotation, a scale factor error correction is possible and a lock-in effect, caused by bias changes in the switching-over of the modulation excursion, is prevented.

TRANSLATED ABSTRACT WORD COUNT: 125

ABSTRACT EP 436052 A1

Zur Vermeidung eines Lock-in-Effekts und zur Vermeidung von Skalenfaktornichtlinearitaten insbesondere bei kleinen Drehraten wird fur einen uber einen digitalen Regelkreis phasenrampenruckgestellten faseroptischen Interferometer-Drehratensensor vorgeschlagen, die zur Gewinnung der Skalenfaktorfehlerinformation erforderliche Umschaltung einer reziproken, alternierenden Phasenverschiebung nicht drehwinkelabhangig, sondern in einem festen Takt vorzunehmen, der vorzugsweise mit der Kreiselmodulationsfrequenz synchronisiert sein kann. Der Vorteil der Erfindung ist, das insbesondere auch bei kleinen Drehraten eine Skalenfaktorfehlerkorrektur moglich und ein Lock-in-Effekt, verursacht durch Bias-Anderungen bei der Modulationshubumschaltung, vermieden wird.

ABSTRACT WORD COUNT: 80

LEGAL STATUS (Type, Pub Date, Kind, Text):

Lapse:	020612	B1	Date of lapse of European Patent in a contracting state (Country, date): ES 19920923, NL 19920923, SE 19920923,
Application:	910710	A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	910710	A1	Date of filing of request for examination: 901217
Examination:	911218	A1	Date of despatch of first examination report: 911031
Grant:	920923	B1	Granted patent
Lapse:	930421	B1	Date of lapse of the European patent in a Contracting State: SE 920923
Lapse:	930526	B1	Date of lapse of the European patent in a Contracting State: NL 920923, SE 920923
Oppn None:	930915	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): German; German; German

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	651
CLAIMS B	(German)	EPBBF1	518
CLAIMS B	(French)	EPBBF1	685
SPEC B	(German)	EPBBF1	5147
Total word count - document A			0
Total word count - document B			7001
Total word count - documents A + B			7001

...CLAIMS operating modes (A, B) in time with the frequency f(sub 0) a

reciprocal alternating **phase shift** ((phi)(sub(M))) of the two counter-rotating light beams, and
- a second signal component...

...0) or integral multiples of t(sub 0), and amplitude increments which compensate nonreciprocal incremental **phase shifts** of the two light beams,
- the amplified **photodetector** output signal (VD(min)) is fed to a first synchronous demodulator (SYNCD1) **clocked** with the frequency f(sub 0),
- the demodulated and amplified output signal (VA) is fed to an **analog** -to- **digital** converter (AD) and after digitization integrated in a **digital** integrator (M(sub 1), ADD1, M2) and is applied to the phase modulator (AM) via a **digital** -to- **analog** converter (DA) and a driver amplifier (AP), in order to compensate nonreciprocal **phase shifts** of the light beams by means of the second signal component,
- a scale factor correction **circuit** is provided which demodulates the amplified **photodetector** output signal (VD(min)) in time with the mode reversal and transmits an **analog** scale factor correction signal (SIA) to the **digital** -to- **analog** converter (DA) via an integrating amplifier (IA), and in which
- a processor (CPU) supplies the control and synchronization signals for the first synchronous demodulator (SYNCD1), the **analog** -to- **digital** converter (AD) and the **digital** integrator (M1, ADD1, M2),

wherein
- between the **digital** integrator (M1, ADD1, M2) and the **digital** -to- **analog** converter (DA) there is arranged a **digital** adder (ADD2) to which at a second input the modulation deviation signal that can be...

...operating modes (A or B) is applied from a first pulse generator (GEN1) that is **clocked** with the frequency f(sub 0) and is set up to transmit to the second input of the **digital** adder (ADD2) a signal corresponding to the phase deviation (+-)(pi)/4 for the first operating...

17/5,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00397818
Charge coupled device imager having multichannel read-out structure
Ladungsgekoppelte Abbildungsanordnung mit Mehrkanallesestruktur
Dispositif de prise de vue a CCD ayant une structure de lecture multicanal
PATENT ASSIGNEE:
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INVENTOR:
Iizuka, Tetsuya, c/o Sony Corporation 7-35 Kitashinagawa 6-chome, Shinagawa-ku Tokyo, (JP)
Yonemoto, Kazuya, c/o Sony Corporation 7-35 Kitashinagawa 6-chome, Shinagawa-ku Tokyo, (JP)
Wada, Kazushi, c/o Sony Corporation 7-35 Kitashinagawa 6-chome, Shinagawa-ku Tokyo, (JP)
Nakamura, Satoshi, c/o Sony Corporation 7-35 Kitashinagawa 6-chome,

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Harada, Koichi, c/o Sony Corporation 7-35 Kitashinagawa 6-chome, Shinagawa-ku Tokyo, (JP)
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PATENT (CC, No, Kind, Date):	EP 383519	A2	900822 (Basic)
	EP 383519	A3	910529
	EP 383519	B1	960605

APPLICATION (CC, No, Date): EP 90301466 900212;
PRIORITY (CC, No, Date): JP 8934569 890214
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G11C-019/28; G11C-027/04; H01L-027/148; H04N-003/15;
CITED PATENTS (EP A): US 4750042 A; US 4750042 A; US 4242692 A; EP 211441 A
CITED REFERENCES (EP A):
IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-13, no. 1, February 1978, pages 34-51; D. BARBE et al.: "Signal processing with charge-coupled devices";

ABSTRACT EP 383519 A2
With the CCD imager of the present invention, signal charges from the image area are transferred by plural juxtaposed read-out registers, through which electrical charges are transmitted, is narrower in width at the image area side and broader in width at the other read-out register side. By virtue of such arrangement of the storage area, there is formed a potential which becomes shallow at the side of the image area and becomes deep at the side of the other read-out registers. By such potential, signal charge transfer efficiency between the read-out registers is improved.
ABSTRACT WORD COUNT: 98

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	900822	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	910529	A3	Separate publication of the European or International search report
Examination:	920102	A2	Date of filing of request for examination: 911105
Examination:	930915	A2	Date of despatch of first examination report: 930803
Grant:	960605	B1	Granted patent
Oppn None:	970528	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	650
CLAIMS B	(English)	EPAB96	653
CLAIMS B	(German)	EPAB96	565
CLAIMS B	(French)	EPAB96	736
SPEC A	(English)	EPABF1	2435
SPEC B	(English)	EPAB96	2642
Total word count - document A			3085
Total word count - document B			4596
Total word count - documents A + B			7681

...SPECIFICATION horizontal registers is phase-shifted by 180(degree) with respect to the other. With the **CCD** imager 41 of the present embodiment, however, signals having the same phase are outputted. Thus the signals

outputted from output buffers 60, 61 of the **CCD** 41 are not subjected to half-bit synchronizing or coinciding treatment and are thus of...

...other. The signals from the output buffers 60, 61 are processed by correlated double sampling **circuits** (CDS) 42, 43 before being converted from the **analog** state into the **digital** state by an A/D converter 44. When the signals are outputted in this manner without coincidizing treatment, a **clock** CL(sub 1) can be used in common in the correlated double sampling **circuits** 42, 43. The same can apply for the **clock** CL(sub 2) supplied to the A/D converter 44. This helps eliminate the problem...

...coupling and relieves the load which would be caused by generation of a number of **clock** types. A frame memory 45 is provided to receive the output of the A/D converter 44. The coinciding can be performed using **clocks** CL(sub 3) and CL(sub 4) supplied to the frame memory 45. In this ...

...SPECIFICATION horizontal registers is phase-shifted by 180(degree) with respect to the other. With the **CCD** imager 41 of the present embodiment, however, signals having the same phase are outputted. Thus the signals outputted from output buffers 60, 61 of the **CCD** 41 are not subjected to half-bit synchronizing or coinciding treatment and are thus of...

...other. The signals from the output buffers 60, 61 are processed by correlated double sampling **circuits** (CDS) 42, 43 before being converted from the **analog** state into the **digital** state by an A/D converter 44. When the signals are outputted in this manner without coincidizing treatment, a **clock** CL(sub(1)) can be used in common in the correlated double sampling **circuits** 42, 43. The same can apply for the **clock** CL(sub(2)) supplied to the A/D converter 44. This helps eliminate the problem...

...coupling and relieves the load which would be caused by generation of a number of **clock** types. A frame memory 45 is provided to receive the output of the A/D converter 44. The coinciding can be performed using **clocks** CL(sub(3)) and CL(sub(4)) supplied to the frame memory 45. In this...

17/5,K/4 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00959044 **Image available**
OPTICAL FIBRE GYRO
GYROMETRE A FIBRE OPTIQUE
Patent Applicant/Assignee:
THALES, 173, boulevard Haussmann, F-75008 Paris, FR, FR (Residence), FR (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
LEHUREAU Jean-Claude, Thales Intellectual Property, 13, av. du Pres. Salvador Allende, F-94117 Arcueil Cedex, FR, FR (Residence), FR (Nationality), (Designated only for: US)
Legal Representative:
BEYLOT Jacques (et al) (agent), Thales Intellectual Property, 13, av. du Pres. Salvador Allende, F-94117 Arcueil Cedex, FR,

Patent and Priority Information (Country, Number, Date):
  Patent: WO 200293110 A1 20021121 (WO 0293110)
  Application: WO 2002FR1503 20020430 (PCT/WO FR0201503)
  Priority Application: FR 20016396 20010515
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
  AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW
  (EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
  (OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
  (AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW
  (EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: G01C-019/72
Publication Language: French
Filing Language: French
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 6083

English Abstract
The invention concerns an optical fibre gyro comprising a Sagnac interferometer using two light waves (S1, S2) circulating in opposite directions in a close-loop waveguide (2), including a **photodetector** (4) delivering an electric signal (Ud) representing the light intensity of disturbances between the two waves, and means for optical **phase - shift** (5) of waves controlled by a slot modulation signal (Um) capable of controlling an optical **phase - shift** variation at a frequency F0 substantially equal to t"sub"0, wherein t"sub"0 is the travel time of a wave in the guide (2). The **photodetector** (5) is connected to at least first (34) and second (36) sampling **circuits** controlled in phase opposition by a **clock** (30) at frequency F0 and supplying two samples (A, B) at each period respectively on a first and a second differential amplifier input (64), an **analog** -to- **digital** converter (42) at the differential amplifier output (42) and an adder/subtractor (46) to accumulate numerical values successively supplied by the **analog** -to- **digital** converter (42). The gyro comprises means (28) for inverting, at a frequency much lower than the frequency F0 the **clock** phase (30) so as to alternate, at frequency f, the direction of the difference of samples at the differential amplifier output, the adder/subtractor (46) is likewise controlled at frequency f, to operate alternately as adder or as subtractor.

French Abstract
La presente invention se rapporte a un gyrometre a fibre optique comprenant un interferometre de Sagnac utilisant deux ondes lumineuses (S1, S2) circulant en sens opposes dans un guide d'onde (2) en anneau, comprenant un photodetecteur (4) delivrant un signal electrique (Ud) representant l'intensite lumineuse des interferences entre les deux ondes, et des moyens de dephasage (5) optique des ondes commandes par un signal de modulation (Um) en creneaux apte a commander une variation de phase optique a une frequence F0 sensiblement egale a a.t0? est le temps de trajet d'une onde dans le guide (2). Le photodetecteur (5) est relie a au moins un premier (34) et un second (36) circuit d'echantillonnage controles en opposition de phase par une horloge (30) a frequence F0 et fournissant deux echantillons (A, B) a chaque periode respectivement sur

une premiere et une seconde entree d'un amplificateur differentiel (64), un convertisseur analogique-numerique (42) a la sortie de l'amplificateur differentiel et un additionneur/soustracteur (46) pour accumuler les valeurs numeriques successivement fournies par le convertisseur analogique-numerique (42). Le gyrometre comporte un moyen (28) pour inverser, a une frequence f tres inferieure a la frequence F0, la phase de l'horloge (30), de maniere a alterner, a la frequence f, le sens de la difference d'echantillons a la sortie de l'amplificateur differentiel, l'additionneur/soustracteur (46) est egalement commande par la frequence f, pour fonctionner alternativement en additionneur ou en soustracteur.

Legal Status (Type, Date, Text)
Publication 20021121 A1 With international search report.
Publication 20021121 A1 Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

English Abstract
...waves (S1, S2) circulating in opposite directions in a close-loop waveguide (2), including a **photodetector** (4) delivering an electric signal (Ud) representing the light intensity of disturbances between the two waves, and means for optical **phase - shift** (5) of waves controlled by a slot modulation signal (Um) capable of controlling an optical **phase - shift** variation at a frequency F0 substantially equal to t"sub"0, wherein t"sub"0 is the travel time of a wave in the guide (2). The **photodetector** (5) is connected to at least first (34) and second (36) sampling **circuits** controlled in phase opposition by a **clock** (30) at frequency F0 and supplying two samples (A, B) at each period respectively on a first and a second differential amplifier input (64), an **analog** -to- **digital** converter (42) at the differential amplifier output (42) and an adder/subtractor (46) to accumulate numerical values successively supplied by the **analog** -to- **digital** converter (42). The gyro comprises means (28) for inverting, at a frequency much lower than the frequency F0 the **clock** phase (30) so as to alternate, at frequency f, the direction of the difference of...

17/5,K/5 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00862546 **Image available**
OPTICAL PROCESSOR ENHANCED RECEIVER ARCHITECTURE (OPERA)
ARCHITECTURE DE RECEPTEUR AVANCEE AVEC PROCESSEUR OPTIQUE (OPERA)
Patent Applicant/Assignee:
ESSEX CORPORATION, 9150 Guilford Road, Columbia, MD 21046, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
TURPIN Terry M, 9918 Evergreen Drive, Ellicott City, MD 21042, US, US (Residence), US (Nationality), (Designated only for: US)
LAFUSE James L, 11836 Bright Passage, Columbia, MD 21044, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
CHARTOVE Alex (et al) (agent), Morrison & Foerster LLP, 2000 Pennsylvania Avenue, N.W., Washington, DC 20006-1888, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200195534 A2-A3 20011213 (WO 0195534)
Application: WO 2001US17777 20010601 (PCT/WO US0117777)

Priority Application: US 2000209434 20000602; US 2001766151 20010119
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H04J-013/00
International Patent Class: H04B-001/707; G06E-003/00
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 13413

English Abstract
A method and apparatus for enhancing the receiving and information identification functions of multiple access communications systems by employing one or more optical processors configured as a bank of 1-D correlators. The present invention is particularly useful in a DS/SS CDMA communications system, resulting in a multiuser CDMA system that approaches carrier to noise performance (C/N) as opposed to being limited by multiple access interference (MAI). The correlators are arranged in parallel to detect and/or demodulate the received signal, in conjunction with one or more complex algorithms to perform near-optimum multiuser detection, perform multipath combining and/or perform carrier Doppler compensation. An improved receiver in accordance with the present invention comprises means for receiving a plurality of signals transmitted through a communications channel; signal conversion means for converting the received signals into a form suitable for input to the multichannel correlator; a multichannel optical correlator for identifying the presence of particular waveforms and estimating the relative time delay or delays, carrier frequency offset from expected, RF amplitude and RF phase for each received spread spectrum waveform present in the received plurality of signals; a controller for determining and providing to the optical correlator the appropriate set of reference hypotheses; and one or more receiver algorithms depending on the exact receiver function to be performed.

French Abstract
L'invention concerne un procede et un appareil permettant d'ameliorer les fonctions de reception et d'identification d'informations de systemes de transmission a acces multiple, par l'utilisation d'un ou de plusieurs processeurs optiques configures comme une banque de correlateurs 1-D. La presente invention convient particulierement a un systeme de transmission DS/SS AMRC, qui devient ainsi un systeme AMRC multi-utilisateurs approchant la performance porteuse-bruit (C/N) a la difference d'un systeme limite par l'interference d'acces multiple (MAI). Ces correlateurs sont disposes parallelement de sorte a detecter et/ou demoduler le signal recu, en conjonction avec un ou plusieurs algorithmes complexes pour une detection multi-utilisateurs quasi optimale, une combinaison a canaux multiples et/ou une compensation Doppler de porteuse. Selon ladite invention, un recepteur ameliore comprend un organe concu pour recevoir une pluralite de signaux transmis a travers un

canal de transmission, un organe de conversion de signaux convertissant les signaux recus en une forme adaptee pour etre fournie au correlateur a canaux multiples, un correlateur optique a canaux multiples servant a identifier la presence de formes d'onde particulieres et estimer le ou les retards relatifs, le decalage des frequences porteuses a partir de l'amplitude HF et de la phase HF attendues pour chaque forme d'onde a spectre etale recue presente dans la pluralite de signaux recue, un controleur concu pour definir et fournir au correlateur optique l'ensemble d'hypotheses de reference approprie ainsi qu'un ou plusieurs algorithmes de reception dependant de la fonction de reception exacte a executer.

Legal Status (Type, Date, Text)

Publication	20011213	A2 Without international search report and to be republished upon receipt of that report.
Examination	20020307	Request for preliminary examination prior to end of 19th month from priority date
Search Rpt	20030821	Late publication of international search report
Republication	20030821	A3 With international search report.

Fulltext Availability:
Claims

Claim
... mixers 66, local oscillator 70, phase shift 72 and, low pass filters 74. Conversion via **analog** -to- **digital** converters 50 generates real part 56 of correlation matrix 22 and imaginary part 58 of...with the present invention makes use of a unique characteristic of a certain class of **photosensors** known as Time Delay and Integrate (TDI) sensors diselosed by
23
Bromley et al. (U...
...s). A CCI) comprises a row of electronic charge holding regions known as wells. A **clocking** signal causes the charge, comprising electrons, to sequentially move from one wel'i to the...

...charge contained within the last well, comprising the charge accumulated at each well along the **CCD** row. This characteristic of accumulating charge as it is shified along the CCI) row is...

...source 76 may be a source
24
suitable for generating coherent light, such as a **semiconductor** laser diode, or may be suitable for generating incoherent light such as a light-emitting...the impinging light for the time interval -r equal to the period of the TDI **clock** and adds the charge to any existing charge in that well. After AT integration period...

...to the previous accumulafion. In general, the value in any well n>O, at any **clock** epoch time T, is the value of the integration for the last integration period AT...

...further defined to be
25
-c = TO + KAt (8)
where K is the number of **clock** cycles of At duration that have occurred since the time offset was some initial value...

...Light Modulator component comprises hypothesis mask 80 (depicted in FIG.

6). The Charge Coupled Device (**CCD**) may employ TDI sensor 80 (depicted in FIG. 6). FIG. 8 is a mathematical representation...

...hypothesis and TDI sensor 106. This Second Preferred Architecture may be constructed either using an **analog** mask register or a binary mask register. FIG. 10 illustrates an example of use of an **analog** mask register as hypothesis register 95. In this embodiment, each row of TDI sensor 86 is fabricated with separate detector elements 94, a separate **analog** summation register 100, and additional **analog** CCI) shift register 95 containing time sequential hypothesis values 82. **Analog** multiplier means 96 is also provided to multiply hypothesis value 82 of the m' entry...of binary values. In this embodiment, a binary register is used as hypothesis register 95. **Analog** multiplier means 96 of FIG. 10 is replaced with switching means 102. If m' hypothesis...

...charge of m' detector element 94 to be summed with the mth-l stage of **analog** sunimation register 100. lf m lh hypothesis register value 82 is equal to "O", switching...

...collecting all light
28
beams physically distributed in space and focusing them onto a single **photodetector** element where they produce an output signal proportional to the sum of their intensities. Examples...

17/5,K/6 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00766379 **Image available**
REDUCED POWER, HIGH SPEED, INCREASED BANDWIDTH CAMERA
CAMERA RAPIDE A FAIBLE CONSOMMATION D'ENERGIE ET LARGEUR DE BANDE ACCRUE
Patent Applicant/Assignee:
REDLAKE IMAGING CORPORATION, Suite A, 18450 Technology Drive, Morgan Hill, CA 95037, US, US (Residence), US (Nationality)
Inventor(s):
COLLINS Galen, 2595 Mt. Pleasant Road, San Jose, CA 95148, US
Legal Representative:
JONES Allston L, Peters, Verny, Jones and Biksa, Suite 6, 385 Sherman Avenue, Palo Alto, CA 94306, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 200079786 A1 20001228 (WO 0079786)
Application: WO 2000US13763 20000519 (PCT/WO US0013763)
Priority Application: US 99338046 19990622
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
CA JP
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: H04N-005/335
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 18639

English Abstract

A high speed electronic camera and a method for reducing the power consumed by a CCD array (12) as the image frame rate increases while maintaining the same operational frequency. The camera includes a lens assembly (10) disposed to receive an image and focus it onto a CCD array (12) to be received by an active image receiving area of a first number of lines. The CCD array (12) also has an active image storage area with the first number of lines to save an image transferred from the active image area wherein each image includes a second number of lines with the second number being less than the first number. The power saving is accomplished with a first of vertical image drivers (14) providing a first pulsed signal to the active image receiving area of the CCD (12) with a third number of pulses in the first pulsed signal equal to the second number of lines of the image being written into the active image area, and a second of the vertical image drivers (14) providing a second pulsed signal to the active image storage area of the CCD (12) to store the image from the active image area into the active image storage area with a fourth number of pulses in the second pulsed signal.

French Abstract

L'invention concerne une camera electronique rapide et un procede de reduction de l'energie consommee par une matrice CCD (12) a mesure que la frequence de trames d'images augmente tout en maintenant la meme frequence operationnelle. La camera comprend un ensemble objectif (10) dispose pour recevoir une image et la focaliser sur une matrice CCD (12) permettant la reception par une zone de reception d'image active d'un premier nombre de lignes. La matrice CCD (12) presente egalement une zone de memorisation d'image active avec le premier nombre de lignes afin de sauvegarder une image transferee par la zone d'image active dans laquelle chaque image comprend un second nombre de lignes, le second nombre etant inferieur au premier nombre. L'economie d'energie est obtenue avec un premier circuit des circuits d'attaque (14) d'images verticales fournissant un premier signal pulse a une zone de reception d'image active de la matrice CCD (12) avec un troisieme nombre d'impulsions dans le premier signal pulse egal au second nombre de lignes de l'image inscrite dans la zone d'image active, et un second circuit des circuits d'attaque (14) d'images verticales fournissant un second signal pulse a la zone de stockage d'images actives de la matrice CCD (12) pour stocker l'image provenant de la zone d'image active dans la zone de stockage d'image active avec un quatrieme nombre d'impulsions dans le second signal pulse.

Legal Status (Type, Date, Text)
Publication   20001228 A1 With international search report.

Fulltext Availability:
  Detailed Description

Detailed Description
... signals from the two channels are automatically demultiplexed with the individual color pixels being in **digital** form. This results from one channel of the **CCD** array providing a RGRG data signal of the image with the **analog** to **digital**0 conversion splitting that signal into a RED data signal and a GRNI data signal. Similarly, the other channel of the **CCD** array provides a GBGB data signal of the image with the **analog** to **digital** conversion splitting the GBGB data signal into a GRN2 data signal and a BLU data signal between the half frequency **clock** and sample **clock** signals, together with the polarity of that difference. This difference signal is integrated to provide an **analog** signal that is proportional to the

phase difference. Additionally, there is a D/A converter...

...to the control subsystem of the camera to receive a signal corresponding to the desired **phase shift** of a particular variable **phase shifter circuit** and convert that **phase shift** signal to an **analog** signal. Finally, there is an operational amplifier coupled to receive the **analog** difference signal from the integrator and the said **analog phase shift** signal from the D/A converter, and coupled to the active filter delay **circuit** to create a voltage feedback signal that adjusts the phase delay presented by the variable **phase shifter circuit** .

There are several other features of the present invention that are needed due to the...

17/5,K/7 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00535358 **Image available**
HIGH SPEED, INCREASED BANDWIDTH CAMERA
CAMERA ULTRARAPIDE A LARGEUR DE BANDE ACCRUE
Patent Applicant/Assignee:
REDLAKE IMAGING CORPORATION,
Inventor(s):
CARROLL Gus F,
COLLINS Galen,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9966710 A1 19991223
Application: WO 99US13702 19990616 (PCT/WO US9913702)
Priority Application: US 9899910 19980618
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AU CA JP AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: H04N-003/14
International Patent Class: H04N-007/01; H04N-005/217
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 17770

English Abstract
Many improvements for a high speed camera including being able to process image data from a **CCD** array (12) at one-quarter the pixel rate at which that image is provided by the **CCD** array (12); automatically demultiplexing color information in the **digital** domain; a **phase shift clock circuit** (26') to individually adjust the phase of the **clock** signal to each A/D converter; high frequency, high power **analog** , bipolar **clock** drivers to drive the horizontal functions of the **CCD** array (12); a technique to minimize the smearing of partial values of previous pixels into later pixels since the **CCD** array (12) is being **clocked** faster than the internal time constant of the output stage of the **CCD** array (12); determination of, and compensation for, the dark reference offset the pixel data streams from the **CCD** array (12); substracting the dark reference offset from the data pixel signal stream from the **CCD** array (12) to stabilize the operating point of the output

amplifier following the **CCD** array (12).

French Abstract

La presente invention se rapporte a de nombreuses ameliorations apportees a une camera ultrarapide: possibilite de traiter un image numerique d'une matrice CCD (12) a un quart du debit pixel selon lequel cette image est formee par la matrice CCD (12); demultiplexer automatiquement les informations couleurs dans le domaine numerique; un circuit d'horloge a dephasage compense (26') pour caler individuellement la phase du signal d'horloge de chaque numeriseur; des pilotes d'horloge bipolaire analogiques haute puissance haute frequence permettant de piloter les fonctions horizontales de la matrice CCD (12); un procede permettant de ramener a un minimum l'effet de traine imputable aux valeurs partielles des pixels anterieurs debordant dans des pixels plus recents, pour la raison que la matrice CCD (12) est synchronisee sur une base de temps plus rapide que la base de temps interne de l'etage de sortie de la matrice CCD (12); determination et correction du decalage du niveau de noir des trains de donnees de pixels provenant de la matrice CCD (12); et enfin, soustraction de ce decalage de niveau de noir dans le train de pixels numerises provenant de la matrice CCD (12), de facon a stabiliser le centrage de l'amplificateur de sortie monte derriere la matrice CCD (12).

English Abstract

...improvements for a high speed camera including being able to process image data from a **CCD** array (12) at one-quarter the pixel rate at which that image is provided by the **CCD** array (12); automatically demultiplexing color information in the **digital** domain; a **phase shift clock circuit** (26') to individually adjust the phase of the **clock** signal to each A/D converter; high frequency, high power **analog** , bipolar **clock** drivers to drive the horizontal functions of the **CCD** array (12); a technique to minimize the smearing of partial values of previous pixels into later pixels since the **CCD** array (12) is being **clocked** faster than the internal time constant of the output stage of the **CCD** array (12); determination of, and compensation for, the dark reference offset the pixel data streams from the **CCD** array (12); substracting the dark reference offset from the data pixel signal stream from the **CCD** array (12) to stabilize the operating point of the output amplifier following the **CCD** array (12). ...

17/5,K/8 (Item 5 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

00523686 **Image available**

OPTICAL COMMUNICATIONS NETWORK

RESEAU DE COMMUNICATIONS OPTIQUE

Patent Applicant/Assignee:
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  COTTER David,
  ELLIS Andrew David,
Inventor(s):
  COTTER David,
  ELLIS Andrew David,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9955038 A1 19991028
  Application: WO 99GB1159 19990415 (PCT/WO GB9901159)

Priority Application: GB 988491 19980421; GB 9812162 19980605
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Main International Patent Class: H04L-007/00
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 17518

English Abstract
An optical regenerator, for example at a node in an optical communications network, uses a free-running bit-asynchronous local clock source. An incoming packet may be used to gate the clock source. In some implementations, a number of gates are used with different delays on the control input, and the gate giving a correctly regenerated output is selected. In alternative embodiments, a control loop is used to adjust the phase of control signals applied to a gate.

French Abstract
On decrit un regenerateur qui, au niveau d'un noeud d'un reseau de communications optique par exemple, met en oeuvre une source d'horloge locale non asservie, asynchrone au niveau du bit. Un paquet entrant peut etre utilise pour servir de porte a la source d'horloge. Dans certaines formes d'execution, un certain nombre de portes sont utilisees avec differents retards a l'entree des instructions et la porte ayant produit une sortie correctement regeneree est choisie. Dans d'autres formes d'execution, une boucle de regulation est utilisee pour regler la phase de signaux de commande appliques a une porte.

Fulltext Availability:
Claims

Claim
... 1 9 are idealised, because it was assumed that all four optical paths between the **clock** source and the output of the selector switch S are precisely equal. These results give...

...regenerators, as shown in Figure 19, in each of which the optical paths between the **clock** source and the output of the selector switch S differ in delay time from the...E) denotes the set JEN,/E
Single Gate Regenerator
In an alternative embodiment, the local **clock** pulse source is again continuously free-running, but requires only one gate to modulate the output of the **clock** pulse source so as to regenerate the packet. The principle of this alternative approach is...

...the free-running local pulse source and the incoming packet. This information is used to **shift** by an appropriate amount the **phase** of the control signal that is applied to the gate. The effect of the **phase** **shifter** is that when a packet data bit of value 1 causes the gate window to open, the window is located as near as possible centrally over

control the **phase shifter** . The control signal to the **phase shifter** may be either an **analogue** or **digital** signal (preferably a **digital** signal at the packet level), and this control signal WO 99/55038 PCT/GB99/01159...

...systematic errors and drift, even if the phase detector is nonlinear. Furthermore, drifts in the **phase shifter** are automatically compensated for by the closed loop (because the **phase shifter** is inside the feedback path). Because, in a practical system, the feedback delay may be...

...The description above includes a discussion of the allowable amount of frequency difference between the **clock** at the packet source and the **clock** in the
asynchronous ...frequency difference between the bit rate of the incoming packet and the full-rate optical **clock** source in the regenerator is significantly smaller than the effective bandwidth of the control loop (including the electronic bandwidth, the feedback delay and the speed of response of the **phase shifter**). Following normal engineering practice, the frequency offset should be at least an order of magnitude...

...Figure 4, and it is assumed that Ms = MI@ = 10).
In an alternative embodiment, the **phase shifter** shown in Figure 25, consisting of DFB laser, switching device UNI1, optical filter F3 and...

...the relatively slow variations in the phase difference between the incoming packets and the local **clock** , rather than abrupt packet-to-packet phase variations. The control loop may therefore be relatively...
...be controlled), i.e. ' 1 Hz, which is a severe restriction. Therefore a motor-controlled **phase shifter** may not have sufficient speed of response for this application. Another type of variable optical and distant **clocks** .
CLAIMS

1 A method of operating a node in an optical communications network including
a...

17/5,K/9 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00296755 **Image available**
MODULAR LASER GYRO
GYROSCOPE A LASER MODULAIRE
Patent Applicant/Assignee:
HONEYWELL INC,
Inventor(s):
KILLPATRICK Joseph E,
BERNDT Dale F,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9514906 A2 19950601
Application: WO 94US13689 19941129 (PCT/WO US9413689)
Priority Application: US 93161555 19931129
Designated States:

(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AU BR CA CN JP KR NO RU AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Main International Patent Class: G01C-019/66
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 36640

English Abstract
A modular laser gyro incorporating a laser gyro with a digital control processor. The digital control processor safely and quickly starts the laser gyro. The microprocessor also executes tests on the gyro and provides a health signal. Optional start-up operations may be performed including the calibration of volts per mode and system configuration. Various information including gyro parameter load commands, gyro control commands, gyro status commands, and gyro calibration and diagnostic commands may be provided to an inertial navigation system. A high voltage start circuit includes a high voltage start module and high voltage pulse generator apparatus. The high voltage start circuit is contained within a modular laser gyro housing. A direct digital dither drive for a dither motor controls the dithering of the gyro to prevent lock in of the laser beams. A dither stripper controls the stripping of the dither signal. A bias drift rate improvement system, as well as a random drift rate improvement system reduces errors. A lifetime prediction mechanism incorporates a memory model that stores worst case performance parameters and evaluates them against predetermined failure criteria. An active current control controls lasing current to prolong life and enhance performance. A single transformer power supply powers the modular gyro.

French Abstract
L'invention concerne un gyroscope a laser modulaire comprenant un gyroscope a laser dote d'un processeur de commande numerique qui demarre ce dernier rapidement et en toute securite. Ledit microprocesseur execute egalement des essais sur le gyroscope et produit un signal de sante. Des operations de demarrage optionnelles, y compris l'etalonnage des volts par mode et la configuration du systeme, peuvent etre realisees. Diverses informations telles que des instructions de charge des parametres relatifs au gyroscope, des instructions de commande du gyroscope, des instructions d'etats du gyroscope ainsi que des instructions d'etalonnage et de diagnostic du gyroscope peuvent etre fournies a un systeme de navigation inertielle. Un circuit de demarrage haute tension situe dans un boitier de gyroscope a laser modulaire comporte un module de demarrage haute tension et un appareil generateur d'impulsions haute tension. Un circuit d'attaque d'oscillation numerique direct pour moteur d'oscillation commande l'oscillation du gyroscope de maniere a empecher le verrouillage des faisceaux laser. Un dispositif de suppression des oscillations commande la suppression du signal d'oscillation. Un systeme d'augmentation de la vitesse de derive de polarisation ainsi qu'un systeme d'augmentation de la vitesse de derive aleatoire permettent de reduire les erreurs. Un mecanisme de prevision de la duree de vie comporte un modele de memoire qui est utilise pour stocker les parametres de performance les pires et les evaluer selon des criteres de defaillance predetermines. Une commande de courant actif regule le courant laser pour prolonger la vie de l'equipement et en augmenter les performances. Le gyroscope modulaire est alimente par une seule alimentation par transformateur.

Fulltext Availability:

Claims

Claim

... an A/D serial data line 2378, a chip select line 2380 and a system **clock** line 2382. The A/D control logic 2348 also receives the sample request line 2390...notdither signal introduce a small displacement in mirror position by AC coupling a small 90' **phase shifted** signal into transducer A associated with mirror 13 only. This enables the **circuit** of Figures 39 and 40 to lock in on a local maximum. The smart mode acquisition brings the **circuit** close to the local maximum LIM signal 20 and the dither part of the **circuit** locks in on the exact peak. The dither and notdither signal results in a small modulation in the power signal from the **photodetector** 160. This small modulation shows up as an AC component on top of the 0...The sweep down and sweep up of the path length controllers are accomplished using the - **circuit** of Figures 39 and 40 where the path length controllers are adjusted accordingly. The process...

18/5,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00862546 **Image available**
OPTICAL PROCESSOR ENHANCED RECEIVER ARCHITECTURE (OPERA)
ARCHITECTURE DE RECEPTEUR AVANCEE AVEC PROCESSEUR OPTIQUE (OPERA)
Patent Applicant/Assignee:
ESSEX CORPORATION, 9150 Guilford Road, Columbia, MD 21046, US, US (Residence), US (Nationality), (For all designated states except: US)
Patent Applicant/Inventor:
TURPIN Terry M, 9918 Evergreen Drive, Ellicott City, MD 21042, US, US (Residence), US (Nationality), (Designated only for: US)
LAFUSE James L, 11836 Bright Passage, Columbia, MD 21044, US, US (Residence), US (Nationality), (Designated only for: US)
Legal Representative:
CHARTOVE Alex (et al) (agent), Morrison & Foerster LLP, 2000 Pennsylvania Avenue, N.W., Washington, DC 20006-1888, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200195534 A2-A3 20011213 (WO 0195534)
Application: WO 2001US17777 20010601 (PCT/WO US0117777)
Priority Application: US 2000209434 20000602; US 2001766151 20010119
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ
EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR
LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL
TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Main International Patent Class: H04J-013/00
International Patent Class: H04B-001/707; G06E-003/00
Publication Language: English
Filing Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 13413

English Abstract
A method and apparatus for enhancing the receiving and information identification functions of multiple access communications systems by employing one or more optical processors configured as a bank of 1-D correlators. The present invention is particularly useful in a DS/SS CDMA communications system, resulting in a multiuser CDMA system that approaches carrier to noise performance (C/N) as opposed to being limited by multiple access interference (MAI). The correlators are arranged in parallel to detect and/or demodulate the received signal, in conjunction with one or more complex algorithms to perform near-optimum multiuser detection, perform multipath combining and/or perform carrier Doppler compensation. An improved receiver in accordance with the present invention comprises means for receiving a plurality of signals transmitted through a communications channel; signal conversion means for converting the received signals into a form suitable for input to the multichannel correlator; a multichannel optical correlator for identifying the presence of particular waveforms and estimating the

relative time delay or delays, carrier frequency offset from expected, RF amplitude and RF phase for each received spread spectrum waveform present in the received plurality of signals; a controller for determining and providing to the optical correlator the appropriate set of reference hypotheses; and one or more receiver algorithms depending on the exact receiver function to be performed.

French Abstract
L'invention concerne un procede et un appareil permettant d'ameliorer les fonctions de reception et d'identification d'informations de systemes de transmission a acces multiple, par l'utilisation d'un ou de plusieurs processeurs optiques configures comme une banque de correlateurs 1-D. La presente invention convient particulierement a un systeme de transmission DS/SS AMRC, qui devient ainsi un systeme AMRC multi-utilisateurs approchant la performance porteuse-bruit (C/N) a la difference d'un systeme limite par l'interference d'acces multiple (MAI). Ces correlateurs sont disposes parallelement de sorte a detecter et/ou demoduler le signal recu, en conjonction avec un ou plusieurs algorithmes complexes pour une detection multi-utilisateurs quasi optimale, une combinaison a canaux multiples et/ou une compensation Doppler de porteuse. Selon ladite invention, un recepteur ameliore comprend un organe concu pour recevoir une pluralite de signaux transmis a travers un canal de transmission, un organe de conversion de signaux convertissant les signaux recus en une forme adaptee pour etre fournie au correlateur a canaux multiples, un correlateur optique a canaux multiples servant a identifier la presence de formes d'onde particulieres et estimer le ou les retards relatifs, le decalage des frequences porteuses a partir de l'amplitude HF et de la phase HF attendues pour chaque forme d'onde a spectre etale recue presente dans la pluralite de signaux recue, un controleur concu pour definir et fournir au correlateur optique l'ensemble d'hypotheses de reference approprie ainsi qu'un ou plusieurs algorithmes de reception dependant de la fonction de reception exacte a executer.

Legal Status (Type, Date, Text)
Publication 20011213 A2 Without international search report and to be republished upon receipt of that report.
Examination 20020307 Request for preliminary examination prior to end of 19th month from priority date
Search Rpt 20030821 Late publication of international search report
Republication 20030821 A3 With international search report.

Fulltext Availability:
Claims

Claim
... and are implemented in conventional digital or analog technology. The advantage of this operation is **reduction** of possible **noise** imparted by optical multichannel correlator 30. The architecture of multichannel optical correlator 30 may be...

...mixers 66, local oscillator 70, phase shift 72 and, low pass filters 74. Conversion via **analog** -to- **digital** converters 50 generates real part 56 of correlation matrix 22 and imaginary part 58 of...with the present invention makes use of a unique characteristic of a certain class of **photosensors** known as Time Delay and Integrate (TDI) sensors diselosed by
23
Bromley et al. (U...

23/5,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00934466
Programmable clock generator for an imaging device
Programmierbarer Taktgenerator fur Abbildungsvorrichtung
Generateur d'horloge programmable pour un dispositif de prise d'images
PATENT ASSIGNEE:
EASTMAN KODAK COMPANY, (201212), 343 State Street, Rochester, New York 14650, (US), (applicant designated states: AT;BE;CH;DE;DK;ES;FI;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
INVENTOR:
Charneski, David M., Eastman Kodak Company, Patent Legal Staff, 343 State Street, Rochester, New York 14650-2201, (US)
Petilli, Eugene M., Eastman Kodak Company, Patent Legal Staff, 343 State Street, Rochester, New York 14650-2201, (US)
Endsley, Jay E., Eastman Kodak Company, Patent Legal Staff, 343 State Street, Rochester, New York 14650-2201, (US)
LEGAL REPRESENTATIVE:
Parent, Yves et al (17684), KODAK INDUSTRIE, Departement Brevets, CRT - Zone Industrielle, 71102 Chalon-sur-Saone Cedex, (FR)
PATENT (CC, No, Kind, Date): EP 851676 A2 980701 (Basic)
EP 851676 A3 990728
APPLICATION (CC, No, Date): EP 97204020 971219;
PRIORITY (CC, No, Date): US 777430 961230
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: H04N-005/335;

ABSTRACT EP 851676 A2
An imaging device for generating an image signal includes an image sensing device for producing an image signal subject to one or more clock signals and means for generating one or more of the clock signals, wherein the clock signal generating means is responsive to a programmable input signal for adjusting a duty cycle of at least one of the clock signals. In particular, by **clocking** two recirculating **shift** registers out of **phase** and parallel loading them with a programmable bit pattern to produce the output clock signals, the frequency of an input clock that is required to produce the output clock signals can be reduced by half.
ABSTRACT WORD COUNT: 109

LEGAL STATUS (Type, Pub Date, Kind, Text):

Withdrawal:	001011	A2	Date application deemed withdrawn: 20000129
Application:	980701	A2	Published application (A1with Search Report ;A2without Search Report)
Search Report:	990728	A3	Separate publication of the European or International search report
Change:	990728	A2	Title of invention (German) (change)

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9827	302
SPEC A	(English)	9827	2880
Total word count - document A			3182
Total word count - document B			0
Total word count - documents A + B			3182

...ABSTRACT adjusting a duty cycle of at least one of the clock signals. In

particular, by **clocking** two recirculating **shift** registers out of **phase** and parallel loading them with a programmable bit pattern to produce the output clock signals...

...SPECIFICATION of this application.

FIELD OF THE INVENTION

The invention relates generally to the field of **digital** integrated **circuits** , and in particular to the generation of periodic signals useful in **digital** integrated **circuits** . More specifically, the invention relates to the generation of clock signals for an imaging device.

BACKGROUND OF THE INVENTION

In **digital** integrated **circuits** which must produce a wide variety of signal patterns, it is often necessary to design...

...of this application is in the field of digital imaging, where a charge coupled device (**CCD**) imager is employed in much the same manner as traditional silver-halide film. A **CCD** imager is a digital device which usually requires a substantial number of input signals with...

...necessary to be able to slightly alter the duty cycle and/or phase of these **CCD** clocks. Specifically, it is desirable to be able to alter pulse width and pulse location within each pixel period. Traditionally, this has been accomplished with **analog** delay **circuits** , synchronous **digital** techniques and/or ad hoc approaches. The disadvantages of these approaches are significant. The **analog** delay **circuits** are expensive and often inaccurate. Most of the digital techniques require high frequency crystal oscillators...

...also result in undesirable levels of radiated electromagnetic interference. Rapid prototyping of these higher speed **circuits** with programmable logic is often impossible, thus forcing engineers to commit their designs to more expensive ASIC (Application Specific Integrated **Circuit**) technology before they have had the opportunity to test them in the system environment. Most...as output by an inverter 48. As a consequence, the registers 40 and 42 are **clocked** out of **phase** with the output of one **shift** register or the other being updated every half period of the PIX(underscore)CLK(underscore...

...the clock generator 12 for as many clock signals as are required to operate the **image** **sensor** 14. The microprocessor 28 would accordingly provide corresponding clocking PATTERN signals and control signals for these additional clock generator **circuits** .

In operation, as shown in the timing diagram of Figure 1B, both PATTERN(underscore)A...which said clock generation means uses a shift register.

An imaging device in which said **clock** generator means uses multiple **shift** registers clocked out of **phase** .

An imaging device where said **shift** register has a programmable modulo.

A clock generator for generating one or more clock signals...

...each shift register responsive to a parallel input of a programmable bit pattern; means for **clocking** the **shift** registers out of **phase** ; and a logic section having inputs connected to corresponding sections of each shift register for shift register.

An apparatus in which said **clock** generator means includes multiple **shift** registers clocked out of **phase** .
An apparatus where said **shift** register has a programmable modulo.
An apparatus where said shift registers each have a programmable...

...shift register
64 inverter
66 set of OR gates
68 set of AND gates
70 **shift** register
72 **phase** locked loop
74 input pattern
76 phase multiplexer
78 modulo multiplexer

...CLAIMS a recirculating configuration.
4. An imaging device as claimed in claim 1 in which said **clock** generator means includes multiple **shift** registers clocked out of **phase** .
5. An imaging device as claimed in claim 4 in which said programmable input signal...

...a recirculating configuration.
8. An imaging device as claimed in claim 1 in which the **clock** generation means includes a **shift** register coupled into a **phase** locked loop having a pair of inputs, said shift register having a clock input and...

23/5,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00832815
DIGITAL OFFSET CORRECTOR FOR MICROBOLOMETER ARRAY
DIGITALE OFFSETKORREKTUR FUR MIKROBOLOMETERMATRIX
CORRECTEUR NUMERIQUE DE DECALAGE POUR MATRICE DE MICROBOLOMETRES
PATENT ASSIGNEE:
Lockheed Martin IR Imaging Systems, Inc., (1308081), 2 Forbes Road, Lexington, MA 02173, (US), (Proprietor designated states: all)
INVENTOR:
BUTLER, Neal, R., 144 School Street, Acton, MA 01720, (US)
LEGAL REPRESENTATIVE:
de Beaumont, Michel (39718), 1, rue Champollion, 38000 Grenoble, (FR)
PATENT (CC, No, Kind, Date): EP 835586 A2 980415 (Basic)
EP 835586 B1 020116
WO 9701926 970116
APPLICATION (CC, No, Date): EP 96921797 960628; WO 96US11014 960628
PRIORITY (CC, No, Date): US 496026 950628
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H04N-005/33
CITED PATENTS (EP B): EP 534769 A; WO 94/00950 A; US 4752694 A
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant:	020116 B1	Granted patent
Application:	970502 A1	International application (Art. 158(1))
Oppn None:	030108 B1	No opposition filed: 20021017

Application: 980415 A2 Published application (Alwith Search Report ;A2without Search Report)
Examination: 980415 A2 Date of filing of request for examination: 980120
Examination: 990623 A2 Date of despatch of first examination report: 990507

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200203	1607
CLAIMS B	(German)	200203	1496
CLAIMS B	(French)	200203	1867
SPEC B	(English)	200203	13573
Total word count - document A			0
Total word count - document B			18543
Total word count - documents A + B			18543

...SPECIFICATION element output.

Until the present invention, focal plane array offset correction has been limited to **analog circuits** that attempt to subtract a real time or stored analog signal from a detected signal...illustrated in FIG. 19;

FIG. 21 is a schematic block diagram of the 90(degree) **phase shifter** illustrated in FIG. 19;

FIG. 22 is a schematic block diagram of an alternate embodiment... comparator 20. The output drivers 148 provide digital data 495 to the off focal plane **circuits** . The **digital** data 495 is a concatenation of the overflow counter and the analog-to-digital converter...provides the analog signal 301 representing the four bit digital number.

Figure 7 shows a **circuit** schematic diagram of one embodiment of an offset controller as may be employed in the...

...and focal plane overflow data 355. The focal plane data 351 is provided for each **image sensor** element of the array, i.e. each bolometer pixel. The focal plane overflow data 355...each transfer latch (latches 26A and 26B being illustrated) and is read by multiplexer readout **circuit** 59.

The **analog** signal on line 181A, the signal to be converted, is stored by capacitor 180A until...arisen when the digital signal on bus 62 was latched by output signal 22A from **analog** comparator 20A. **Circuit** analysis of this latch train arrangement has indicated that the metastability of the system is...

...bus 62.

The high speed clock 64 is also connected to a 90(degree) analog **phase shifter** 42. The 90(degree) **phase shifter** 42 generates the least significant bit signal, LSB 60, as part of the digital Gray...

...by delaying the 75 MHZ clock by precisely 90(degree), 1/4 of a complete **clock** cycle, in closed loop **phase shifter** 42. This type of **phase shifter** is sometimes referred to as a delay locked loop.

Reference is now made to FIG...

...to FIG. 21, which FIG. is a schematic block diagram of the 90(degree) analog **phase shifter** 42 illustrated in FIG. 19. High speed clock 64 and its complement from clock multiplier...of the circuit of FIG. 19. In the circuit of FIG. 6, the 90(degree) **phase shifter** 42 of FIG. 3 has been eliminated. In addition, clock multiplier 50 has been modified...

...in connection with FIG. 4.
VCO 94 also provides a second output 95 that is **phase shifted** 90(degree) with respect to output 89 and then provided to another squaring circuit 90...
...of the CMOS invertor, the propagation delay increases as the supply voltage is decreased.
The **phase shift** per stage in the ring oscillator is:
For example, in the five stage oscillator illustrated in FIG. 24, the **phase shift** per stage is 36(degree). Thus, a tap two stages away from the main output will have a 72(degree) **phase shift**, while a tap three stages away from the main output will have a 108(degree) **phase shift**. If all of the invertors are identical, then a 90(degree) **phase shift** is not possible.
However, if the different invertors in the ring oscillator are not identically constructed, then a 90(degree) **phase shift** between invertors in the ring oscillator can be obtained. In a CMOS invertor, the delay...

...the remaining invertors in the ring can be used to provide the required 90(degree) **phase shift**.
In VCO 94 illustrated in FIG. 24, the propagation delay of invertor 98 is adjusted...

...delay through modified invertor 98 and invertor 99, then there is exactly a 90(degree) **phase shift** between outputs 89 and 95.
Reference is now made to FIG. 25, which FIG. is...speed clock could be used to control counter 48, flip-flop 44, and 90(degree) **phase shifter** 42.
One advantage of the present invention is that the Gray code least significant bit...Each converter itself needs only a sample and hold, a comparator, and an array of **digital** latches.
The **circuits** of the present invention may be monolithically integrated in semiconductor form using convention CMOS technology...

...CLAIMS second compensation signal (763).
14. The apparatus of claim 13, wherein the second offset compensation **circuit** includes:
a **digital** -to-analog converter (144) to receive digital offset data (353) and to output an analog...

23/5,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00377387
Electronic camera with proofing feature.
Elektronische Kamera mit Prufvorrichtung.
Camera electronique avec dispositif de verification.
PATENT ASSIGNEE:
EASTMAN KODAK COMPANY (a New Jersey corporation), (201210), 343 State Street, Rochester New York 14650, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Bell, Cynthia Sue c/o Eastman Kodak Company, Patent Department 343 State Street, Rochester New York 14650, (US)
LEGAL REPRESENTATIVE:
Parent, Yves et al (17681), Kodak-Pathe Departement Brevets et Licences

Centre de Recherches et de Technologie Zone Industrielle, F-71102 Chalon-sur-Saone Cedex, (FR)

PATENT (CC, No, Kind, Date): EP 356351 A1 900228 (Basic)
EP 356351 B1 931020

APPLICATION (CC, No, Date): EP 89420300 890810;

PRIORITY (CC, No, Date): US 234788 880822

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: H04N-005/76; H04N-005/907;

CITED PATENTS (EP A): US 4262301 A; US 4604668 A; US 4714962 A

ABSTRACT EP 356351 A1

A camera (10) comprised of an electronic imager (52) and a plurality of display/frame stores (14(sub 1)-14(sub(n))). Each of the plurality of display/frame stores (14(sub 1)-14(sub(n))) is individually selectable, for example, by a transparent touch-sensitive media (40) positioned over the plurality of display stores (14(sub 1)-14(sub(n))). The selection acts to either retain or to discard the displayed image. Retained images may be downloaded to an optional memory module (76) in the camera (10) or to a larger, non-integral, data base/printer (24) for providing finished photos of the images selected for saving. An auxiliary storage may be attached to expand the number of images that may be retained prior to downloading.

ABSTRACT WORD COUNT: 117

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	900228	A1	Published application (A1with Search Report ;A2without Search Report)
Examination:	900905	A1	Date of filing of request for examination: 900713
Examination:	920805	A1	Date of despatch of first examination report: 920619
Grant:	931020	B1	Granted patent
Oppn None:	941012	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	1142
CLAIMS B	(German)	EPBBF1	486
CLAIMS B	(French)	EPBBF1	704
SPEC B	(English)	EPBBF1	3899
Total word count - document A			0
Total word count - document B			6231
Total word count - documents A + B			6231

...SPECIFICATION each display frame to retain only those images desired by the photographer.

Electronic cameras using **solid state image sensing** devices **such as a charge** coupled device (**CCD**) have been receiving increased **interest** as a potential replacement for the universally accepted silver halide film type camera. Within the...control logic block 72 forms a part of a controller 70. An imager timing control **circuit** **55** receives a fixed frequency signal from an oscillator 54. The timing control **circuit** 55 also receives the picture enable signal PK, from the control logic block 72. The...

...a clock bus 59. The voltage translator 53, in response to the clock signal CLK, **provides** various clocking and control signals to the **image** **sensor** 52 to activate the **sensor** to store the optical image impinging on the sensor. The various clocking and control signals are

shown in Figures 5 and 6. Output signals from the **image sensor** 52 are amplified by an amplifier 56 and are directed to a sample and hold **circuit** 57. The sample and hold **circuit** also receives the CLK signal from **the image** timing control **circuit** 55 over the clock bus 59. A threshold adjust **circuit** 58 receives the output from the sample and hold **circuit** 57 and operates to provide a black level **clamp to** the signals. The imaging signals from the threshold adjust **circuit** 58 are then directed to **an** A/D converter 110. The **A** /D converter 110 also receives the clocking signal CLK and **provides** at its output the digitized version of the signals **appearing** at its input.

The output of the A/D **converter** 110 is connected to an image data bus 100. A multiple image display subsystem 80 is shown comprised of, **a** plurality of image display and storage devices 14(sub 1) through 14(sub(n)) and...a manner consistent with the transfer of imagewise charge and depends on the type of **image sensor** . For example, with a two-phase **CCD** (charge-coupled device) or BBD (bucket brigade device) the clockouts are accomplished by rapid sequential clocking of a horizontal shift register (not shown part of **CCD image sensor chip**). The sequential clocking is shown in Figure 5 as E and F, (PHI)H1 and (PHI)H2. These are the picture element rate clocks. When **the last** element of the horizontal **shift register has** been **clocked** out, the next row of picture elements (pixels) are transferred in parallel into the horizontal shift register. This transfer is accomplished by stopping **the horizontal clocks as** shown in Figure 5, C and D. The two phases of vertical gates, A and...

...rate clocks are shown in B and C. The output driver (not shown part of **CCD image sensor chip**) is reset to a reference voltage prior to each pixel measurement. The reset clock is...

...level is sampled at timing indicated by the (PHI)C, waveform denoted E in Figure **6 . The output voltage** showing these steps is denoted G. Following the reset and settling of the output driver...

...voltage will reflect that intensity. The fact sheets supplied by EASTMAN KODAK COMPANY with their **image sensor** contains the schematic and timing diagrams which describe the previously discussed shift registers and waveforms...

...with switch 19 being placed in the ON position. A user I/O (in/out) **instruction module** 201 is activated directing the user, through prompt codes displayed by the instruction panel 62...loaded the answer from block 409 will be YES which in turn will enable the **chip select** for **the** desired display via block 410 which in turn will set the display write enable terminal...

23/5,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00217342
Television apparatus Pix-in-Pix.
Fernsehapparat Bild im Bild.
Appareil de television a image dans l'image.
PATENT ASSIGNEE:
RCA LICENSING CORPORATION, (944400), 2 Independence Way, Princeton New

Jersey 08540, (US), (applicant designated states: AT;DE;FR;GB;IT;SE)
INVENTOR:
Christopher, Todd J., 1402 South Kitley Avenue, Indianapolis Indiana 46203, (US)
LEGAL REPRESENTATIVE:
Pratt, Richard Wilson et al (46454), London Patent Operation G.E. TECHNICAL SERVICES CO. INC. Burdett House 15/16 Buckingham Street, London WC2N 6DU, (GB)
PATENT (CC, No, Kind, Date): EP 200330 A1 861105 (Basic)
EP 200330 B1 910612
APPLICATION (CC, No, Date): EP 86302022 860319;
PRIORITY (CC, No, Date): US 715818 850325
DESIGNATED STATES: AT; DE; FR; GB; IT; SE
INTERNATIONAL PATENT CLASS: H04N-005/44; H04N-005/262; H04N-009/74;
CITED PATENTS (EP A): US 4267560 A; DE 2937133 A; US 4298891 A
CITED REFERENCES (EP A):
FUNK-TECHNIK 40 (1985), No. 10, Heidelberg HELMUT MITSCHKE "Ein Fernsehgerat fur mehrere Videosignale" Pages 409-410
page 410, column 1, line 22
column 2, line 9
fig. 4;

ABSTRACT EP 200330 A1
A pix-in-pix television display includes circuitry for reducing the amount of memory needed to hold one field of the reduced size image. In the display apparatus, digital samples representing the large (40) and small picture (10) signals are developed at substantially equal rates by separate circuitry (40,10) Subsampling circuitry (14,16,18,22) stores one out of every five of the samples representing a horizontal line of the small picture. These samples are displayed, synchronous with the large picture (26,34,36) at a rate three-fifths times the display rate of the large picture samples to produce an apparent size reduction of one-third in the horizontal direction.
ABSTRACT WORD COUNT: 106

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	861105	A1	Published application (A1with Search Report ;A2without Search Report)
*Search Report:	870204	A1	Separate publication of European or Intl search report (change)
*Application:	870204	A1	Date and kind of publication of European patent application (change):
Examination:	870923	A1	Date of filing of request for examination: 870708
Change:	880608	A1	Representative (change)
*Assignee:	880608	A1	Applicant (transfer of rights) (change): RCA LICENSING CORPORATION (944400) 2 Independance Way Princeton New Jersey 08540 (US) (applicant designated states: AT;DE;FR;GB;IT;SE)
*Assignee:	880608	A1	Previous applicant in case of transfer of rights (change): RCA CORPORATION (209202) 201 Washington Road Princeton, NJ 08540 (US) (applicant designated states: AT;DE;FR;GB;IT;SE)
Examination:	890906	A1	Date of despatch of first examination report: 890725
Grant:	910612	B1	Granted patent
Change:	920401	B1	Representative (change)
Oppn None:	920603	B1	No opposition filed

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	2469
CLAIMS B	(German)	EPBBF1	1188
CLAIMS B	(French)	EPBBF1	1717
SPEC B	(English)	EPBBF1	12033
Total word count - document A			0
Total word count - document B			17407
Total word count - documents A + B			17407

...SPECIFICATION converter before being stored in a dynamic RAM which forms a field memory although a **CCD** or BBD memory could be used instead. The number of samples formed and stored corresponds...

...samples are read-out at twice the write-in rate.
In US-A-4249213 the **area** reduction in auxiliary image size is to 1/9th of the main image. "One line...

...7 is a block diagram of a memory output address and clock signal generator suitable **for use** in the receiver shown in FIGURE 1.
FIGURE 8 is a timing diagram that is...may be required in certain of the signal paths. One skilled in the art of **digital circuit** design would know where such delays would be needed in a particular system.
FIGURE 1...

...Y(sub(A)) and C(sub(A)) are applied to the pix-in-pix subsampling **and** synchronizing **circuitry** 11. Subsampling and synchronizing circuitry 11 reduces the information content of both the luminance, Y...

...sequential lines of the main signal.
Auxiliary luminance and chrominance samples from circuitry 11 are **applied** to the **digital** -to-analog converter (DAC) and matrix circuit 36. The DAC and matrix circuit 36 converts the auxiliary **digital** luminance and chrominance signals to respective analog signals and combines them in appropriate proportions to...

...second set of input terminals of multiplexer 38.
Multiplexer 38 responsive to a signal, MUX **CONTROL** , from **circuitry** 11, selectively, alternately applies the main color signals from source 40 and the auxiliary color...the viewer control 413, and a value of 0 or 2 is stored in the **PHASE register** depending on whether WCLK/2 is low or high when the first pulse of the...the end of the four clock period in which the control data is loaded into **shift** register 622, **clock** generator 624 is preset to the phase value for the line. Clock generator 624 is...

23/5,K/5 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00375070 **Image available**
UNCOOLED FOCAL PLANE ARRAY SENSOR
CAPTEUR DE MOSAIQUE DE PLAN FOCAL NON REFROIDIE
Patent Applicant/Assignee:
LOCKHEED-MARTIN IR IMAGING SYSTEMS INC,
MARSHALL Charles M,
BUTLER Neal R,

Inventor(s):
  MARSHALL Charles M,
  BUTLER Neal R,
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9715813 A1 19970501
  Application: WO 96US17028 19961024 (PCT/WO US9617028)
  Priority Application: US 95547344 19951024
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
  AL AM AT AU AZ BA BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IL IS
  JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO
  RU SD SE SG SI SK TJ TM TR TT UA UG US UZ VN KE LS MW SD SZ UG AM AZ BY
  KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF
  BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: G01J-005/10
International Patent Class: G01J-05:20; H04N-05:33
Publication Language: English
Fulltext Availability:
  Detailed Description
  Claims
Fulltext Word Count: 12801

English Abstract
A staring focal plane array sensor includes optics located along an optical path, for transmitting radiation. A focal plane array and integrated circuit, located along the optical path for receiving the transmitted radiation, responsively produces image signals from the transmitted radiation. The integrated circuit includes apparatus for converting the image signals into digital image data at digital image data outputs.

French Abstract
Ce capteur de mosaique de plan focal sans balayage comprend une optique situee le long d'un trajet optique, aux fins d'emission d'un rayonnement. Une mosaique de plan focal et un circuit integre, places sur le trajet optique aux fins de reception du rayonnement emis, produisent en reponse des signaux d'image a partir du rayonnement emis. Le circuit integre comprend un dispositif de conversion des signaux d'image en donnees d'images numeriques au niveau des sorties de donnees d'images numeriques.

Fulltext Availability:
  Detailed Description

Detailed Description
... data, and creates a real time visible display. It is also desirable to have a **sensor** wherein **images** are created with the use of a microbolometer focal plane array having a digital image data output integrated into I 0 a single **chip** , processing electronics, power supply and display.

Summary Of The Invention
The present invention provides a...

...uncooled focal plane array sensor comprising a microbolometer focal plane array integrated into a semiconductor **circuit** with a **digital** image output in a package of modular construction having smaller size, lighter weight, and lower...15;

RECTIFIED SHEET (RULE 91)
FIG. 17 is a schematic block diagram of the 90' **phase shifter** illustrated in FIG. 15; FIG. 18 is a schematic block diagram of an alternate embodiment...

...I 00 converts the radiation to electronic signals that are read out and digitized by **analog** -to- **digital circuitry** integrally constructed on an integrated circuit chip, where the integrated circuit chip also comprises the...comparator 20. The output drivers 148 provide digital data 495 to the off focal plane **circuits** . The **digital** data 495 may be clocked with the pixel clock.

In the example embodiment, a bolometer...each transfer latch (latches 1026A and 1026B being illustrated) and is read by multiplexer readout **circuit** 1059.

The **analog** signal on line 10 I 5A, the signal to be converted, is stored by capacitor...arisen when the digital signal on bus 1062 was latched by output signal 1022A from **analog** comparator 1020A. **Circuit** analysis of this latch train arrangement has indicated that the metastability of the system is...on bus 1062.
The high speed clock 1064 is also connected to a 90' analog **phase shifter** 1042. The 900 **phase shifter** 1042 generates the least significant bit signal, LSB 1060, as part of the digital Gray...

...is generated by delaying the 75 MHZ clock by precisely 90', 1/4of a complete **clock** cycle, in closed loop **phase shifter** 1042. This type of **phase shifter** is sometimes referred to as a delay locked loop.

Reference is now made to FIG...FIG. 17, which figure is a schematic block diagram of the 90' 1 5 analog **phase shifter** 1042 illustrated in FIG. 15. High speed clock 1064 and its complement ftom clock multiplier...

...embodiment of the circuit of FIG. 15. In the circuit of FIG. 18, the 90' **phase shifter** 1042 of FIG.

15 has been eliminated. In addition, clock multiplier 1050 ...in connection with FIG. 16.

VCO 10120 also provides a second output 10122 that is **phase shifted** 90' with respect to 1 5 output 10108 andthen providedto another squaring circuit 10110. Squaring...
...of the CMOS inverter, the propagation delay increases as the supply voltage is decreased.

The **phase shift** per stage in the ring oscillator is.

(2) Phase/stage = 180/p
For example, in the five stage oscillator illustrated in FIG. 20, the **phase shift** per stage is 36'. Thus, a tap two stages away from the main output will have a 721 **phase shift** , while a tap three stages away
RECTIFIED SHEET (RULE 91)
- 21 from the main output will have a 108' **phase shift** . If all of the inverters are identical, then a 90' **phase shift** is not possible.

However, if the different inverters in the ring oscillator are not identically constructed, then a 90' **phase shift** between invertors in

the ring oscillator can be obtained. In a CMOS ...to the remaining inverters in the ring can be used to provide the required 90' **phase shift** .

In VCO 120 illustrated in FIG. 20, the propagation delay of inverter 10130 is adjusted...
...inverter 10 1 30 and inverter 10 1 32, then there is exactly a 90' **phase shift** between 1 5 outputs 10108 and 10122.

Reference is now made to FIG. 21, which...high speed clock could be used to control counter 1048, flip-flop 1044, and 90' **phase shifter** 1042.

One advantage of the present invention is that the Gray code least significant bit...Each converter itself needs only a sainple and hold, a comparator, and an array of **digital** latches.

The **circuits** of the present invention may be monolithically integrated in semiconductor form using convention CMOS technology...

23/5,K/6 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00361601 **Image available**
DIGITAL OFFSET CORRECTOR FOR MICROBOLOMETER ARRAY
CORRECTEUR NUMERIQUE DE DECALAGE POUR MATRICE DE MICROBOLOMETRES
Patent Applicant/Assignee:
LOCKHEED MARTIN IR IMAGING SYSTEMS,
BUTLER Neal R,
Inventor(s):
BUTLER Neal R,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9701926 A2 19970116
Application: WO 96US11014 19960628 (PCT/WO US9611014)
Priority Application: US 95496026 19950628
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG US UZ VN KE LS MW SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: H04N-005/33
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 15511

English Abstract
An offset corrector for a focal plane array. A bolometer array configured in a row and column readout format has dedicatad column circuits to measure the resistance of each bolometer in the column. A high speed on-**chip analog** to **digital** converter converts the analog sensor signal to a digital representation. Since the response of each bolometer varies, an offset controller, connected to the output of the analog to digital converter, corrects the digital representation for variations in

individual bolometer response. Each pixel has a corresponding dynamically computed offset stored in an offset memory. The offset is computed when a chopper or shutter blocks radiation from the local plane array. The focal plane array is temperature stabilized to a predetermined temperature to keep bolometer response within a predetermined bandwidth.

French Abstract

Correcteur de decalage pour matrice de plan focal. Une matrice de bolometres configuree en un format d'affichage en rangees et colonnes presente des circuits de colonnes specialises destines a mesurer la resistance de chaque bolometre dans la colonne. Un convertisseur analogique-numerique rapide sur puce convertit le signal du capteur analogique en une representation numerique. Etant donne que la reponse de chaque bolometre varie, un controleur de decalage, connecte a la sortie du convertisseur analogique numerique, corrige la representation numerique des variations dans une reponse de bolometre individuel. Chaque pixel presente un decalage correspondant calcule de maniere dynamique, stocke dans une memoire de decalage. Le decalage est calcule lorsqu'un decoupeur ou un obturateur bloque le rayonnement provenant de la matrice de plan focal. La matrice de plan focal est stabilisee en temperature a une temperature predeterminee afin de maintenir la reponse des bolometres a l'interieur d'une largeur de bande predeterminee.

Fulltext Availability:
Detailed Description
Claims

English Abstract

...circuits to measure the resistance of each bolometer in the column. A high speed on- **chip** **analog** to **digital** converter converts the analog sensor signal to a digital representation. Since the response of each...

Detailed Description

... element output.

Until the present invention, focal plane array offset correction has been limited to **analog** **circuits** that attempt to subtract a real time or stored analog signal from a detected signal...loop illustrated in FIG. 19;
FIG. 21 is a schematic block diagram of the 90' **phase** **shifter** illustrated in FIG. 19; FIG. 22 is a schematic block diagram of an alternate embodiment...comparator 20. The output drivers 148 provide digital data 495 to the off focal plane **circuits** . The **digital** data 495 is a concatenation of the overflow counter and the analog-to-digital converter...provides the analog signal 301 representing the four bit digital number.

Figure 7 shows a **circuit** schematic diagram of one embodiment of an offset controller as may be employed in the...and focal plane overflow data 355. The focal plane data 351 is provided for each **image** **sensor** element of the array, i.e. each bolometer pixel. The focal plane overflow data 355...each transfer latch (latches 26A and 26B being illustrated) and is read by multiplexer readout **circuit** 59.
The **analog** signal on line 15A, the signal to be converted, is stored by capacitor 23A until...arisen when the digital signal on bus 62 was latched by output signal 22A from **analog** comparator 20A. **Circuit** analysis of this latch train arrangement has indicated that the metastability of the system is 90' analog **phase** **shifter** 42. The 90' **phase** **shifter** 42 generates the least significant bit signal, LSB 60,

23/5,K/7 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00358966 **Image available**
ELECTRO-OPTICAL STEP-FRAME CAMERA SYSTEM WITH IMAGE MOTION COMPENSATION
SYSTEME ELECTRO-OPTIQUE DE PHOTOGRAPHIE IMAGE PAR IMAGE A COMPENSATION DE FILAGE

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Patent and Priority Information (Country, Number, Date):
Patent: WO 9641480 A1 19961219
Application: WO 96US8736 19960604 (PCT/WO US9608736)
Priority Application: US 95486989 19950607
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG US UZ VN KE LS MW SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Main International Patent Class: H04N-007/18
International Patent Class: H04N-09:47
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 11920

English Abstract
An electro-optical step-frame camera system in which succesive overlapping frames of scene imagery are generated by an electro-optical imaging array, and in which electronic image motion compensation is performed by the array during the generation of at least some of the frames of imagery (100). The succesive frames of imagery are made in a stepping pattern that is repeated in a series of cycles of steps, each step separated by a framing interval in which a frame of imagery is obtained (142). The stepping cycles of the camera generate sweeping coverage of the terrain of interest. As the velocity of height to ratio of the reconnaissance aircraft changes, the stepping cycle and electronic image motion compensation are continually adjusted, so as to ensure maximum scene coverage and preservation of image resolution (24).

French Abstract
Systeme electro-optique de photographie image par image a compensation de filage dans lequel une mosaique electro-optique genere des images consecutives, qui se chevauchent, correspondant a l'imagerie d'une scene et realise la compensation electronique de filage durant la generation

d'au minimun quelques images (100). Les images consecutives sont prises selon le schema d'echelonnement repete en une serie de cycles d'echelonnement, chaque echelon etant separe du suivant par un intervalle de cadrage durant lequel une image est prise (142). Les cycles d'echelonnement de l'appareil generent un balayage du terrain observe. La vitesse changeant en fonction de l'altitude de l'avion de reconnaissance, le cycle d'echelonnement et la compensation electronique de filage sont regles en continu, de facon a assurer le maximum de couverture de la scene et la conservation de la resolution de l'image (24).

Fulltext Availability:
Detailed Description

Detailed Description
... 38, lens housing 104 and lens 40, in alignment with the lens axis LA. An **image sensor** unit (ISU) 60 is placed directly behind the array 32. The **image sensor** unit 60 includes the camera control computer 34, the drive and control electronics **circuitry** 54, the signal processing **circuitry** 56, and the master clock 58, which are all discussed in detail below. Fans 63 cirulate air in the camera housing 38 and **image sensor** unit 60. Incident light comes through a
window 128, where it is reflected off mirror...14 along the line AA'. The polysilicon horizontal lines 72 are pulsed by the 3- **phase clocks** substrate 71 to be **shifted** down the array. In FIG. 15, the polysilicon horizontal lines 72 are isolated from each...the spirit and scope of the invention as defined in the appended claims. For example, **digital** electronic control **circuits** other than those disclosed can be used to control the charge transfe rates in the column groups of an imaging array. Moreover, **analog circuits** , delay **circuits** , or other types of control circuits may be devised to control the charge transfer rates to achieve forward motion compensation. In addition, many of the functions performed by the disclosed **digital** electronic control **circuits** can be implemented in software by computer 34 or another data processor. As previously noted...